

Aims of the Conference:

ASP-DAC 2016 is the 21th annual international conference on VLSI design automation in Asia and South Pacific regions, one of the most active regions of design and fabrication of silicon chips in the world. The conference aims at providing the Asian and South Pacific CAD/DA and Design community with opportunities of presenting recent advances and with forums for future directions in technologies related to Electronic Design Automation (EDA). The format of the meeting intends to cultivate and promote an instructive and productive interchange of ideas among EDA researchers/developers and system/circuit/device designers. All scientists, engineers, and students who are interested in theoretical and practical aspects of VLSI design and design automation are welcomed to ASP-DAC.

Areas of Interest:

Original papers in, but not limited to, the following areas are invited.

[1] System-Level Modeling and Design Methodologies:

- 1.1. HW/SW co-design, co-simulation and co-verification
- 1.2. System-level design exploration, synthesis and optimization
- 1.3. Model- and component-based embedded system/software design
- 1.4. System-level formal verification
- 1.5. System-level modeling, simulation and validation tools/methodologies

[2] Embedded System Architectures and Design:

- 2.1. Many- and multi-core SoC architectures
- 2.2. Reconfigurable and self-adaptive SoC architectures
- 2.3. Domain-specific architectures
- 2.4. Dependable architectures
- 2.5. On-chip memory architectures
- 2.6. Cyber physical systems
- 2.7. Storage system architecture
- 2.8. Internet of things

[3] On-chip Communication and Networks-on-Chips:

- 3.1. On-chip communication networks
- 3.2. Networks-on-chips
- 3.3. Interface and I/O design
- 3.4. Optical and RF on-chip communications

[4] Embedded Software:

- 4.1. Kernel, middleware and virtual machines
- 4.2. Compiler and toolchains
- 4.3. Real-time systems
- 4.4. Resource allocation for heterogeneous computing platforms
- 4.5. Storage software and applications
- 4.6. Human-computer interface
- 4.7. System verification and analysis

[5] Device/Circuit-Level Modeling, Simulation and Verification:

- 5.1. Device/circuit/interconnect modeling and analysis
- 5.2. Device/circuit-level simulation tools and methodologies
- 5.3. RTL and gate-level modeling, simulation and verification
- 5.4. Circuit-level formal verification

[6] Analog, RF and Mixed Signals:

- 6.1. Analog/mixed-signal/RF synthesis
- 6.2. Analog/mixed-signal/RF testing
- 6.3. Analog layout verification and simulation techniques
- 6.4. Noise analysis
- 6.5. High-frequency electromagnetic simulation of circuits
- 6.6. Mixed-signal design consideration
- 6.7. Power-aware analog circuit/system design
- 6.8. Analog/mixed-signal modeling and simulation techniques

[7] System-Level Power and Thermal Management:

- 7.1. System-level low-power design and thermal management
- 7.2. System-level power modeling, analysis and simulation
- 7.3. Cross-layer reliability and aging
- 7.4. Architectural low-power design techniques
- 7.5. Energy harvesting and battery management

[8] Device/Circuit/Gate-Level Low Power Design:

- 8.1. Low-power design and methodologies
- 8.2. Power modeling, analysis and simulation
- 8.3. Thermal aware design

[9] Logic/Behavioral/High-Level Synthesis and Optimizations:

- 9.1. High-level synthesis tools and methodologies
- 9.2. Combinational, sequential and asynchronous logic synthesis
- 9.3. Logic synthesis and physical design techniques for FPGAs
- 9.4. Technology mapping

[10] Physical Design:

- 10.1. Floorplanning, partitioning and placement
- 10.2. Interconnect planning and synthesis
- 10.3. Placement and routing optimization
- 10.4. Clock network synthesis
- 10.5. Post layout and post-silicon optimization
- 10.6. Package/PCB/3D-IC routing

[11] Design for Manufacturability and Reliability:

- 11.1. Reticule enhancement, lithography-related design and optimization
- 11.2. Resilience under manufacturing variations
- 11.3. Design for manufacturability, yield, defect tolerance, cost issues, and DFM impact
- 11.4. Reliability, aging and soft error analysis
- 11.5. Design for reliability and robustness

[12] Timing and Signal/Power Integrity:

- 12.1. Deterministic/statistical timing and performance analysis and optimization
- 12.2. Power/ground and package modeling, analysis and optimization
- 12.3. Signal/power integrity, EM modeling and analysis
- 12.4. Extraction, TSV and package modeling
- 12.5. 2D/3D on-chip power delivery network analysis and optimization

[13] Test and Design for Testability:

- 13.1. ATPG, BIST and DFT
- 13.2. Fault modeling and simulation
- 13.3. System test and 3D IC test
- 13.4. Online test and fault tolerance
- 13.5. Memory test and repair
- 13.6. Analog and mixed-signal test

[14] Security and Fault-Tolerant Systems:

- 14.1. Security modeling and analysis
- 14.2. Architectures, tools and methodologies for secure hardware
- 14.3. Design for security and security primitives
- 14.4. Cross-layer security
- 14.5. Fault analysis, detect and tolerance

[15] Emerging Technologies:

- 15.1. New transistor/device and process technologies: spintronic, phase-change, single-electron etc.
- 15.2. CAD for nanotechnologies, MEMS, 3D ICs, quantum computing etc.

[16] Emerging Applications:

- 16.1. Biomedical applications
- 16.2. Big data applications
- 16.3. Advanced multimedia applications
- 16.4. Energy-storage/smart-grid/smart-building design and optimization
- 16.5. Datacenter optimization
- 16.6. Automotive system design and optimization
- 16.7. Electromobility

ACM, IEEE, and IEICE reserve the right to exclude a paper from distribution after the conference (e.g., removal from ACM Digital Library and IEEE Xplore) if the paper is not presented at the conference by the author of the paper. ASP-DAC does not allow double and/or parallel submissions of similar work to any other conferences, symposia, and journals.

Submission of Papers:

Deadline for submission: **5 PM JST (UTC+9), July 8 (Wed), 2015**
Notification of acceptance: **Sep. 14 (Mon), 2015**
Deadline for final version: **5 PM JST (UTC+9), Nov. 9 (Mon), 2015**

For detailed instructions for submission, please refer to the "Authors' Guide" at: <http://www.aspdac.com/aspdac2016/>

ASP-DAC 2016 Chairs

General Chair:

Rui Paulo da Silva Martins (University of Macau, Macao, China)

Technical Program Chair:

Ting Ting Hwang (National Tsing Hua University, Taiwan)

Technical Program Vice Chairs:

David Z. Pan (University of Texas at Austin, USA)

Pui-In Mak (University of Macau, Macao, China)

Panels, Special Sessions, and Tutorials: Suggestions and proposals are welcome and have to be addressed to the Conference Secretariat (aspdac2016-sec@mls.aspdac.com) no later than May 29 (Fri), 2015.

Contact: Conference Secretariat: aspdac2016-sec@mls.aspdac.com TPC Secretariat: aspdac2016-tpc@mls.aspdac.com

Call for Designs

University LSI Design Contest

ASP-DAC 2016

<http://www.aspdac.com/aspdac2016/>
February 1-4, 2016
Macao, China



Aims of the Contest:

As a unique feature of ASP-DAC 2016, the University LSI Design Contest will be held. The aim of the Contest is to encourage education and research on VLSI design at universities and other educational organizations. We solicit designs that fit in one or more of the following categories:

- (1) Designed, and actually implemented on chips in universities or other educational organizations during the last two years;
- (2) Designs that report actual measurements from implementations;
- (3) Innovative design prototypes.

Interesting or excellent designs selected will be honored by providing the opportunities for presentation in a special session at the conference. Award(s) will be given to a few numbers of outstanding designs, selected from those presented at the conference.

Areas of Design:

Application areas or types of circuits of the original LSI circuit designs include (but are not limited to):

- (1) Analog, RF and Mixed-Signal Circuits, (2) Digital Signal Processing, (3) Microprocessors, (4) Custom ASIC.

Methods or technology used for implementation include:

- (a) Custom ASIC and Cell-Based LSIs, (b) Gate Arrays, (c) FPGA/PLDs.

Submission of Design Descriptions:

A camera-ready summary is requested to be prepared within 2 pages including figures, tables, and references. It is strongly recommended that measured experimental results and a chip micrograph are included in the summary. Please do not submit the same paper as a regular paper.

Specification of the submission format will be available at <http://www.aspdac.com/aspdac2016/>

Deadline for summary:	5PM JST (UTC+9) Jul. 8 (Wed.), 2015
Notification of acceptance:	Sep. 14 (Mon.), 2015
Deadline for camera-ready:	5PM JST (UTC+9) Nov. 9 (Mon.), 2015

Review:

Submitted designs will be reviewed by the Design Contest Committee in a process similar to the review process for the technical papers. The following criteria will be applied in the selection of designs:

- (1) Reliability of design and implementation, (2) Quality of implementation, (3) Performance of the design, (4) Novelty of application, algorithm, architecture, (5) Others.

Interesting or excellent designs selected will be presented at a special session of the conference.

Presentation:

An author of each selected design will be required to make a short presentation at a special session of ASP-DAC 2016. A digest of each design to be presented will be included in the conference proceedings.

Contact Email: aspdac2016-udc@mls.aspdac.com

ASP-DAC 2016 Chairs

General Chair:	Rui Paulo da Silva Martins (University of Macau, Macao, China)
Technical Program Chair:	TingTing Hwang (National Tsing Hua University, Taiwan)
Technical Program Vice Chairs:	David Z. Pan (University of Texas at Austin, USA) Pui-In Mak (University of Macau, Macao, China)
Design Contest Co-Chairs:	Mang-I Vai (University of Macau, Macao, China) Man-Kay Law (University of Macau, Macao, China)

Prospective Sponsors: ACM SIGDA, IEEE CASS, IEEE CEDA, Macau Chapter of IEEE CASS