A Single-Branch Third-Order Pole–Zero Low-Pass Filter With 0.014-mm^2 Die Size and 0.8-kHz (1.25-nW) to 0.94-GHz (3.99-mW) Bandwidth–Power Scalability

Yong Chen, *Member, IEEE*, Pui-In Mak, *Senior Member, IEEE*, Stefano D'Amico, Li Zhang, He Qian, and Yan Wang

***Abstract*—A single-branch third-order low-pass filter with an ultracompact die size and extensive bandwidth (BW)–power scalability is described. It unifies a *source follower*, a *stackable floating active inductor*, and a *feedforward capacitor* to constitute a transistorized-LC-ladder topology with a stable pole–zero transfer function over a wide range of tunable BW. Differentially, only eight transistors and five untuned capacitors are required. Fabricated in 0.18-μm CMOS, the prototype occupies 0.014-mm^2 die size. By scaling the bias current (and, hence, the power), the flexible BW measures 0.8 kHz at 1.25 nW and 0.94 GHz at 3.99 mW.**

***Index Terms*—CMOS, low-pass filter (LPF), source-follower-based, stackable floating active inductor (SFAI).**

I. Introduction

MULTISTANDARD transceivers based on software-defined radios favor bandwidth (BW)-scalable low-pass filters (LPFs) to cope with the different types of channel occupying kilohertz (e.g., GSM) to gigahertz (e.g., IEEE 802.11ad WLAN) wide spectrums. However, implementing the flexible-BW LPFs with a wide tuning range, a small die size, and a high intermodulation-free dynamic range (IMFDR) remains very challenging.

A number of techniques have been explored to deal with BW scaling but with a tradeoff between common specifications such as gain, IMFDR, silicon area, and power consumption. Capacitor-array BW adjustment [1], [2] has the benefit of minor impact on the filter's linearity and shape but suffers from an apparent tradeoff among the area, BW coverage, and step size. Also, the power cannot be scaled with the BW for adaptability in the system level. Alternatively, $g_m - C$ LPFs with voltage-based [3] or current-based [4] BW tuning can alleviate such a tradeoff. Both offer continuous and wide-range BW–power scalability excellent for performance-on-demand operation. Nevertheless, most CMOS transconductors [3], [4] suffer from strong noise and linearity penalties when the bias current or supply voltage ($V_{\rm DD}$) is extensively lowered down. Additionally, as common CMOS transconductors are composed of numerous transistors, any inner parasitic pole will penalize their power in high-frequency filtering.

This brief proposes a continuous-time third-order pole–zero LPF with extensive BW–power scalability and compact die area. Unlike the $g_m - C$ LPF in [3] that demands a number of transconductors, the proposed LPF unifies a source follower (SF) and a stackable floating active inductor (SFAI) in a current-reuse branch. Together with the use of a feedforward capacitor around the SFAI, a novel transistorized-LC-ladder topology is realized, achieving a stable pole–zero transfer function over a wide range of tunable BW.

Manuscript received February 27, 2013; revised May 6, 2013, June 26, 2013, and August 4, 2013; accepted August 21, 2013. Date of publication September 30, 2013; date of current version November 14, 2013. This work was supported in part by the National 973 and 863 Programs of China and in part by Macau FDCT. This brief was recommended by Associate Editor H. Barthelemy.

Y. Chen, L. Zhang, H. Qian, and Y. Wang are with the Institute of Microelectronics, Tsinghua University, Beijing 100084, China (e-mail: chenyong@ieee.org).

P.-I. Mak is with the State Key Laboratory of Analog and Mixed-Signal VLSI and FST-ECE, University of Macau, Macao, China (e-mail: pimak@umac.mo).

S. D'Amico is with the Department of Innovation Engineering, University of Salento, 73100 Lecce, Italy (e-mail: stefano.damico@unisalento.it).

Color versions of one or more of the figures in this brief are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2013.2281717

II. SFAI

Instead of cascading a number of biquads for filter-order extension, one can employ the LC-ladder topology to achieve better circuit robustness over process variations. However, common negative-feedback impedance converters [5]–[7] for the required active inductors minimally entail four transconductors, and each draws a separated current. This brief introduces a current-reuse four-transistor one-capacitor SFAI, as depicted in Fig. 1(a). It is built with two positive-feedback (PF) impedance converters ($M_{2p,n}$ and $M_{3p,n}$ with transconductances of g_{m2} and g_{m3}, respectively) connected in series with respect to the medium nodes ($V_{YP,N}$), where there is a differential capacitor ($C_2/2$). The circuit simplicity of this SFAI not only minimizes the parasitic effects but also offers self-biasing and current reusability with other circuitry. $M_{2p,n}$ in cross-diode connection creates a PF impedance converter transferring the capacitive behavior of $C_2/2$ into inductive at $V_{XP,N}$. $M_{3p,n}$ with $C_2/2$ also creates the same inductive effect at $V_{ZP,N}$ while generating a negative resistance ($-2/g_{m3}$) at $V_{XP,N}$, canceling the resistive loss ($2/g_{m2}$) due to $M_{2p,n}$. One can prove that, when the output conductance of each MOSFET is taken into account, the loop gains of the two PF loops around $M_{2p,n}$ and $M_{3p,n}$ are always less than unity, ensuring a stable operation.

Two half-circuit equivalent models [Fig. 1(b) and (c)] are employed to analyze the admittance transformation characteristic of the SFAI. For simplicity, $M_{2p,n}$ and $M_{3p,n}$ are equally sized

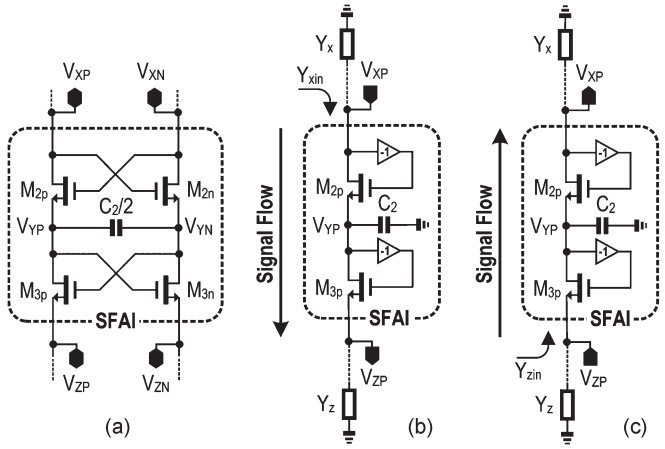

Fig. 1. (a) Proposed four-transistor one-capacitor SFAI. It can be merged with other functions to achieve current reuse. Its bidirectional admittance transformation characteristic: (b) Y_{xin} from V_{XP} to V_{ZP} and (c) Y_{zin} from V_{ZP} to V_{XP}.

and biased for the same transconductance ($g_{m2} = g_{m3} = g_{mL}$) and output resistance ($r_{o2} = r_{o3} = r_{oL}$). The admittance transformation is derived with two opposite signal directions. The first case [Fig. 1(a)] is from V_{XP} to V_{ZP}. When the parasitic admittance (Y_z) at V_{zp} is considered, the input admittance (Y_{xin}) at V_{XP} can be derived

$$Y_{xin} = -g_{mL} + \frac{1}{r_{oL}} + \frac{1}{\frac{sC_2}{g_{mL}^2 - 1/r_{oL}^2} + \frac{2/r_{oL}}{g_{mL}^2 - 1/r_{oL}^2} + \frac{1}{g_{mL} + 1/r_{oL} + Y_z}}. \tag{1}$$

Upon proper sizing, $g_{mL}^2 \gg 1/r_{oL}^2$ is achieved to simplify (1) as

$$Y_{xin} \approx \frac{1}{R_{px}} + \frac{1}{sL_{\rm act} + R_s + R_{pz}//(1/Y_z)} \tag{2}$$

where $L_{\rm act}$ is the equivalent inductance, R_s is the equivalent series resistance, and R_{px} and R_{pz} are the equivalent input and output resistances of the SFAI, respectively.

The second case [Fig. 1(b)] is from V_{ZP} to V_{XP}. When the parasitic admittance (Y_x) at V_{XP} is considered, the input admittance (Y_{zin}) at V_{ZP} can be obtained

$$Y_{zin} = g_{mL} + \frac{1}{r_{oL}} + \frac{1}{\frac{sC_2}{g_{mL}^2 - 1/r_{oL}^2} + \frac{2/r_{oL}}{g_{mL}^2 - 1/r_{oL}^2} + \frac{1}{-g_{mL} + 1/r_{oL} + Y_x}}. \tag{3}$$

Similar to the steps in (1) and (2), we can simplify (3) as

$$Y_{zin} \approx \frac{1}{R_{pz}} + \frac{1}{sL_{\rm act} + R_s + R_{px}//(1/Y_x)}. \tag{4}$$

Equations (2) and (4) together yield the equivalent circuit model and parameters given in Fig. 2. Interestingly, the SFAI and its model are bidirectional valid, i.e., the signal can flow from V_{XP} to V_{ZP} or vice versa. This work employs the former to realize our proposed LPF. According to R_s and $L_{\rm act}$, the quality factor ($Q_{\rm Lact}$) of the SFAI is $Q_{\rm Lact} = \omega r_{oL} C_2/2$, which is, to the first order, independent of g_{mL}, being very suitable for BW scaling.

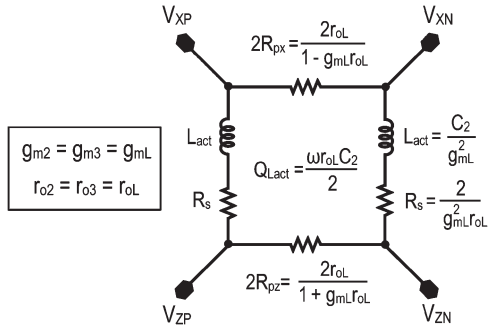

Fig. 2. Equivalent circuit model of the SFAI when $M_{2p,n}$ and $M_{3p,n}$ are equally sized and biased.

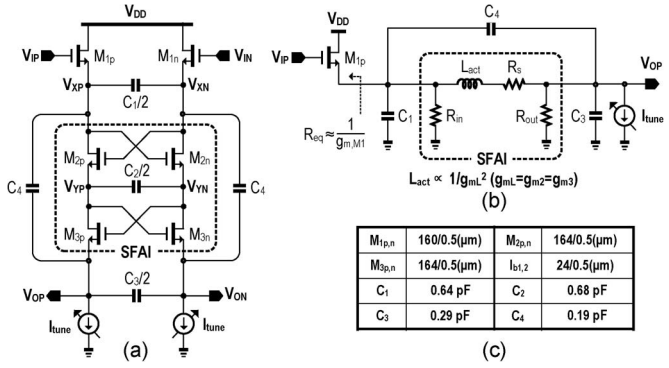

Fig. 3. Proposed single-branch third-order LPF with $I_{\rm tune}$ for BW tuning. (a) Schematic. (b) Half-circuit equivalent model with the SFAI substituted by Fig. 2. (c) Optimized device sizes.

III. Proposed Single-Branch Third-Order LPF

The wide-BW and high-linearity properties of SF-based LPF have been demonstrated in prior works such as [8]. It features an inherently linear I/O transfer characteristic (i.e., $V_{\rm gs}$ of a MOSFET), no inner parasitic pole, and no need of common-mode (CM) feedback in differential realization. The proposed single-branch third-order LPF [Fig. 3(a)] can be considered as an order-extended SF-based LPF. The SF ($M_{1p,n}$) that served as the input stage contributes a $g_{m,M1}$-controllable pole that is linearly tunable by $I_{\rm tune}$. The high input impedance of SF also facilitates the design of its driving circuit. The SF cascoded atop the SFAI ($M_{2p,n}$, C_2, and $M_{3p,n}$) shares the same $I_{\rm tune}$, which is tuned for scaling the BW with the power. The output CM voltage is ($V_{\rm GS1} + V_{\rm GS2} + V_{\rm GS3}$) lower than the input CM voltage. The low output impedance ($2/g_{mL}$) enhances its load drivability. Together with C_1 and C_3, a BW-scalable LC-ladder topology is realized. Elegantly, the complex poles are also linearly tunable with g_{mL} since $L_{\rm act} \propto 1/g_{mL}^2$. A coherent third-order transfer function hence can be achieved over a wide range of tunable BW without the area impact induced by tuning capacitors.

Without the feedforward capacitor C_4, the LPF offers an all-pole transfer function suitable for Butterworth response. With another untuned C_4 added, a tunable stopband zero can be created with a fixed frequency distance to other tunable poles. Thus, it features the same g_{mL} controllability, enhancing the close-in stopband rejection. The resultant pole–zero transfer function thereby can support the Chebychev-II response, as realized in this work.

Fig. 3(b) depicts the half-circuit equivalent of the LPF for analyzing the transfer function. For simplicity, the parasitic

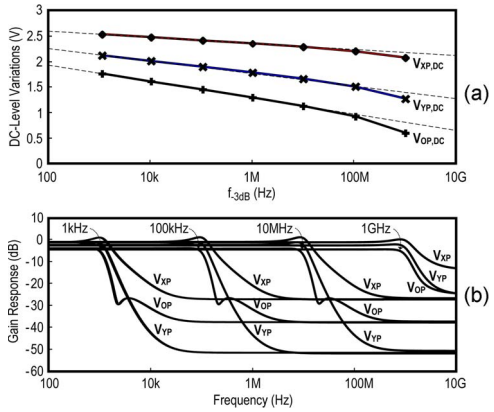

Fig. 4. Simulated CM voltages at V_{XP}, V_{YP}, and V_{OP} with respect to the $f_{-3\mathrm{dB}}$. (b) Simulated gain responses at the internal nodes (V_{XP} and V_{YP}) and output node (V_{OP}) at different $f_{-3\mathrm{dB}}$ values.

capacitances and output resistance of all MOSFETs are ignored at this stage. The parameters in Fig. 3(b) are substituted by $R_s = 0$, $R_{\mathrm{in}} = -1/g_{mL}$, and $R_{\mathrm{out}} = 1/g_{mL}$. The transfer function of this LPF is written as

$$H(s) = A_{\mathrm{dc}} \frac{s^2 b_2 + s b_1 + 1}{s^3 a_3 + s^2 a_2 + s a_1 + 1} \tag{5}$$

where $A_{\mathrm{dc}} = 1$, $b_2 = (C_2 C_4)/(g_{mL}^2)$, $b_1 = 0$

$$\begin{aligned} a_3 &= \frac{C_2}{g_{mL}^2} \frac{C_1 C_3 + C_4(C_1 + C_3)}{g_{m1}} \\ a_2 &= \frac{C_2}{g_{mL}^2} \frac{g_{mL} C_1 + g_{m1} C_4 + (g_{m1} - C_{mL}) C_3}{g_{m1}} \\ a_1 &= \frac{C_2}{g_{mL}^2} \frac{g_{mL}(g_{m1} - C_{mL}) C_2 + C_1(C_1 + C_3) g_{mL}^2}{g_{m1} C_2}. \end{aligned} \tag{6}$$

To enlarge the dynamic range and BW tuning range, an elevated V_{DD} was employed as in [9] and [10], ensuring adequate device overdrive voltages against a wide range of bias current. Operated at a 3-V V_{DD} and due to the self-bias nature of the SFAI, the simulated dc-level variations [Fig. 4(a)] at $V_{XP,N}$, $V_{YP,N}$, and $V_{OP,N}$ are fairly linear with frequency (log) over a wide range of -3-dB cutoff frequency $(f_{-3\mathrm{dB}})$ from 1 kHz to 1 GHz, with the bias current rising from 0.42 nA to 1.33 mA. By defining the safe operating area (SOA) of transistors according to the design rule manual, transient simulations with node-voltage trajectory checks [10] can ensure that no device is over the SOA at all time. The buildup of the filtering profile at different $f_{-3\mathrm{dB}}$ values is shown in Fig. 4(b).

A. DC Gain

The proposed LPF operates like a composite SF with a dc gain ideally equal to unity. However, if the finite output resistance of MOSFET is accounted, A_{dc} is lowered as given by

$$A_{\mathrm{dc}} \approx \frac{\sqrt{2\mu_n C_{\mathrm{ox}} \left(\frac{W}{L}\right)_1}}{\sqrt{2\mu_n C_{\mathrm{ox}} \left(\frac{W}{L}\right)_1} + (\lambda_1 + \lambda_b)\sqrt{I_{\mathrm{tune}}}} \tag{7}$$

where the square-law approximation is applied for generality; $(W/L)_1$ is the input transistor $(M_{1p,n})$ aspect ratio, and λ_1 and λ_b denote the channel-length modulation coefficient of the input and bias current transistors, respectively. Thus, A_{dc} is closer to unity if all MOSFETs are of longer channel length, similar to [8]. Based on (7), A_{dc} will be slightly reduced when the BW is increased. As the described LPF is built by NMOS devices, deep n-well should be required to avoid the body effect (i.e., by body–source connection). The corresponding substrate diodes raise the parasitic capacitance at the inner nodes, lowering the maximum achievable BW. Alternatively, one can compensate the dc gain via proper upsizing the transconductance of the SFAI with respect to that of $M_{1p,n}$, but in this way, the stability must be checked to ensure that all node impedances are still positive against process variations and mismatches.

B. Stopband Zero

If the output resistance of each MOSFET is counted, b_1 in (6) can be recalculated as $b_1 = 2C_4/g_{mL}^2 r_{oL}$, and we can get the frequency (f_{zero}) and quality factor (Q_{zero}) of the stopband zero

$$f_{\mathrm{zero}} = \frac{1}{2\pi}\sqrt{\frac{2\mu_n C_{\mathrm{ox}} \left(\frac{W}{L}\right)_L I_{\mathrm{tune}}}{C_2 C_4}} \quad Q_{\mathrm{zero}} \approx \frac{1}{\lambda_L V_{ovL}}\sqrt{\frac{C_2}{C_4}} \tag{8}$$

where λ_L is the channel-length modulation coefficient and V_{ovL} is the overdrive voltage of the SFAI. Equation (8) also helps to understand the tunability of the stopband zero. Its location should be consistently shifted with other poles, as confirmed by the simulations in Fig. 4(b). V_{ovL} becomes larger with the BW increment, as shown in Fig. 4(a). Accordingly, Q_{zero} will be lowered with frequency, limiting the stopband rejection. This is consistent with the results shown in Fig. 4(b), where the stopband zero starts to vanish with the BW close to $\sim$1 GHz.

C. IRN Voltage

For simplicity, only the thermal noise is analyzed. The input-referred noise (IRN) voltage can be calculated as

$$V_{\mathrm{IRN}}^2 = \frac{8kT\gamma}{\sqrt{I_{\mathrm{tune}}}}\left(1 + \frac{2\sqrt{\beta_L} + \sqrt{\beta_b}}{\sqrt{\beta_1}}\right) \tag{9}$$

where β_L, β_b, and β_1 are the technology parameters $(\mu_n C_{\mathrm{ox}}(W/L))$ for $M_{2p,n}$ to $M_{3p,n}$, the bias current transistor, and $M_{1p,n}$, respectively. When the BW is increased with I_{tune}, the V_{IRN}^2 will be reduced with $\sqrt{I_{\mathrm{tune}}}$.

D. Linearity

At relatively low frequency, similar to [8], the IIP3 of the LPF can be approximated as

$$\mathrm{IIP3} = \frac{16}{\sqrt{3 \cdot \left(\frac{V_{ov1}}{V_{E2}^3} + \frac{V_{ov2}}{V_{E3}^3} + \frac{V_{ov3}}{V_{E4}^3}\right)}} \tag{10}$$

where V_{ov1}, V_{ov2}, and V_{ov3} are the overdrive voltages of M_1, M_2, and M_3, respectively, and V_{E2}, V_{E3}, and V_{E4} are the early voltages of M_2, M_3, and the bias current transistor, respectively. Supposing that $V_{ov1} = V_{ov2} = V_{ov3} = V_{ov}$ and $V_{E2} = V_{E3} = V_{E4} = V_E$, (10) can be simplified as

$$\mathrm{IIP} = \frac{16}{3 \cdot \sqrt{\frac{V_{ov}}{V_E^3}}}. \tag{11}$$

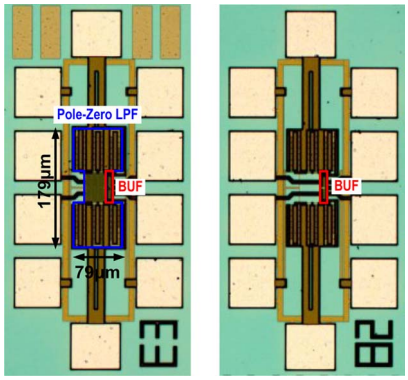

Fig. 5. Die photographs of (left) the pole–zero LPF and (right) its reference path.

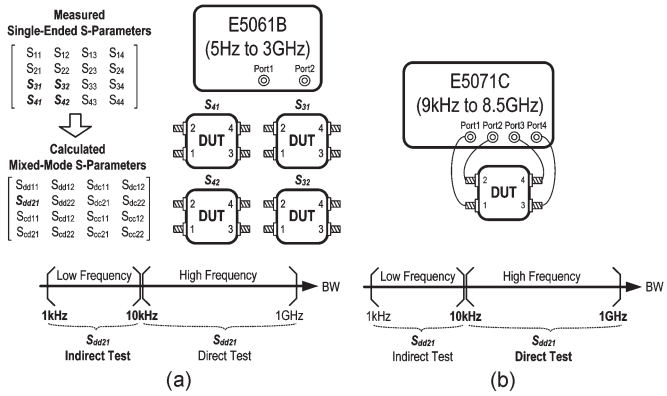

Fig. 6. Experimental setup with network analyzers (E5061B and E5071C) for S_{dd21} measurements: (a) Low frequency and (b) high frequency.

It shows that the IIP3 is improvable by decreasing V_{ov}, which differs from what generally happens in $g_m - C$ LPFs [4], [6], [7]. Thus, for a fixed bias current, decreasing V_{ov} while enlarging the transistor size can increase their transconductance, offering a way to optimize the noise with linearity. Note that an elevated V_{DD} allows not only more V_{GS} and V_{DS} on each device for better linearity but also more voltage swing at the internal and output nodes to enhance the signal-to-noise ratio. The main tradeoff is the power consumption that must be balanced in the design phase and cooptimized in simulations.

IV. Measurement Results

The third-order pole–zero LPF and its reference path with an identical output buffer for de-embedding the LPF's factual performances from the effects of the I/O parasitics and buffer were fabricated in 0.18-μm CMOS. Their chip micrographs are shown in Fig. 5. The core area of the LPF is just 0.014 mm^2. In order to isolate the LPF from the parasitics associated with the PCB, the on-chip test buffers were placed at the same location for both the LPF and its reference path. All MOSFETs are sized sufficiently large with $L = 0.5$ μm (Fig. 3) to optimize the major performance metrics that are quite interdependent for this single-branch LPF. For instance, $M_{2p,n}$ and $M_{3p,n}$ (164/0.5 μm) show large output resistances of 18.21 kΩ at 665 μA and 2.2 GΩ at 208 pA. The simulated $1/f$ corner frequencies are 20 MHz at 665 μA and 4 Hz at 208 pA. Obviously, larger devices induce more parasitic capacitances, limiting the achievable BW and the effectiveness of the added stopband zero. Hence, the channel length is a tradeoff between the accuracy of the frequency response and linearity.

Measuring the differential frequency response (S_{dd21}) from the subkilohertz range to the gigahertz range is nontrivial. Fig. 6(a) and (b) shows the proposed experimental setup. Two network analyzers E5061B and E5071C were employed. The E5071C has a built-in fixture simulator for balanced measurements with four ports for the high-frequency range. This supports direct S_{dd21} measurement by connecting the four ports of the E5071C to the device under test. For the low-frequency range, only the E5061B with two-port option is available to measure the single-ended S-parameters (S_{xy}), but the mixed-mode S-parameters can be indirectly calculated according to [11]. For instance, the single-ended S-parameters (S_{41}, S_{31}, S_{42}, and S_{32}) can be measured according to the connection

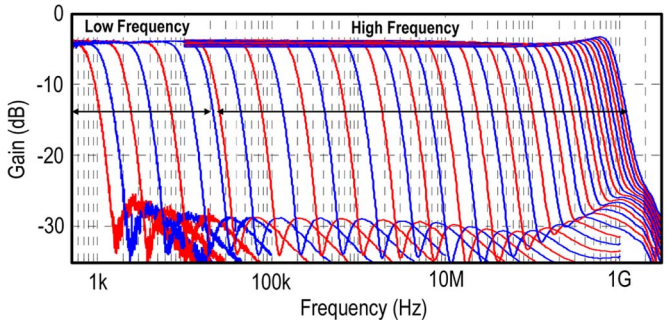

Fig. 7. Measured gain responses.

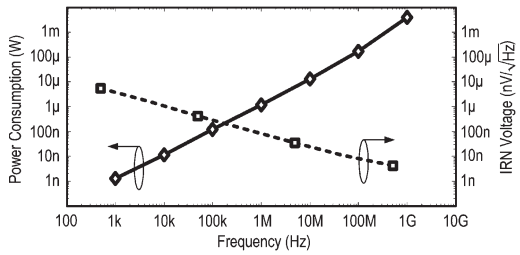

Fig. 8. Power consumption and IRN voltage versus different $f_{-3\mathrm{dB}}$ values.

schemes shown in Fig. 6(a); the frequency response that is the magnitude of the S_{dd21} can be calculated as

$$S_{\mathrm{dd21}} = \frac{1}{2}(S_{31} - S_{41} - S_{32} + S_{42}). \tag{12}$$

Thus, we were able to measure consistent frequency responses in the low-frequency (1–10 kHz) and high-frequency ($>$ 10 kHz) ranges. At the transition edge in Fig. 7, the two closer curves are to show the consistency of all responses with respect to the two methods.

The location of the zeros changes at high frequencies, which is due to the small size of the used capacitors compared with the device parasitics. The measured $f_{-3\,\mathrm{B}}$ is tuned from 0.8 kHz to 0.94 GHz with the power dissipation rising from 1.25 nW to 3.99 mW, as shown in Fig. 8. The measured passband gain varies between -4.7 and -3.7 dB. Their shapes are consistent owing to the concurrent and equal-scale tuning of all poles and zeros via one shared bias current. The slightly increased ripple at the higher BW occurs because the quality factor of the complex poles becomes larger by the bigger parasitic

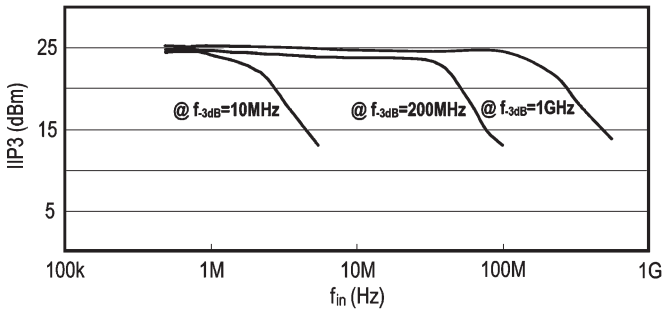

Fig. 9. In-band IIP3 versus $f_{\rm in}$.

TABLE I
CHIP SUMMARY AND BENCHMARK WITH THE STATE OF THE ART

Parameters	This Work	ISSCC'12 [3]	TCASII'11 [4]
Technology	180nm CMOS	65nm CMOS	180nm CMOS
Architecture	SF + SFAI	Gm-C	Gm-C
Order, Type	3rd, Chebychev-II	3rd, Chebychev-I	6th, Butterworth
Power-BW Tradability	(Current ↔ BW)	(V_{DD} ↔ BW)	(Current ↔ BW)
DC Gain (dB)	–4.7 to –3.7	+1.3 to +2.7	0
$IIP3_{In\text{-}band}$ (dBm)	+24 @ $f_{in}=f_{-3dB}/10$ +13 @ $f_{in}=f_{-3dB}/2$	+7 to +8	–9 *
IRN ($V_{rms}/\sqrt{Hz}$) @ f_{-3dB}	5.5μ @ 0.8kHz 4.2n @ 0.94GHz	6.61n @ 4.7GHz 5.02n @ 10GHz	3.8μ @ 100Hz * 142.3n @ 400kHz *
f_{-3dB} Range (Hz)	0.8k to 0.94G	0.6G to 10G	100 to 10M
f_{-3dB} Tunability ($f_{-3dB,max}$ / $f_{-3dB,min}$)	1,175,000	16.7	100,000
Power (W) @ f_{-3dB}	1.25n @ 0.8kHz 3.99m @ 0.94GHz	19m @ 4.7GHz 140m @ 10GHz	36p to 3.6m **
Die Area (mm^2)	0.014	0.01	0.16
V_{DD} (V)	3	1 to 1.4 (tune f_{-3dB} from 4.7 to10GHz)	1.8
FOM_1	0.52p @ 0.8kHz 1.33p @ 0.94GHz	1.34p @ 4.7GHz 4.66p @ 10GHz	60p
FOM_2	226.5	178.3	196.0

* Extracted values from plots ** Calculated from 60pW/Pole/Hz

capacitance at $V_{OP,N}$. The $Q_{\rm zero}$ of the stopband zero also reduces as the BW is increased, as analyzed in Section III-B.

A low-noise differential amplifier (ADL5565) was used to facilitate the noise measurement. After proper de-embedding, the IRN voltage of the LPF measures 5.5 $\mu{\rm V}_{\rm rms}/\sqrt{\rm Hz}$ at a 0.8-kHz $f_{-3\rm dB}$ and 4.2 $\rm nV_{rms}/\sqrt{Hz}$ at a 0.94-GHz $f_{-3\rm dB}$. The IRN variations in Fig. 8 agree well with (9) under the low and high $I_{\rm tune}$ values. The $1/f$ corner frequencies are 10 Hz for a 0.8-kHz $f_{-3\rm dB}$ and 35 MHz for a 0.94-GHz $f_{-3\rm dB}$.

The IIP3 measured at 50 Ω and 10/200/1000-MHz $f_{-3\rm dB}$ is $> +13$ dBm up to 5/100/500-MHz input frequency $(f_{\rm in})$, as shown in Fig. 9. The IIP3 drops when $f_{\rm in}$ gets closer to $f_{-3\rm dB}$. The high-frequency linearity is limited by the nonlinear parasitic capacitances (e.g., $C_{\rm gs}$) of the MOSFETs, confirmed by the transistor-level simulations.

The chip summary and performance benchmark are given in Table I. We employ the $\rm FOM_1 = Power/(}f_{-3\rm dB} \times$ Numbers of Pole) [3] and the more comprehensive $\rm FOM_2$ [7] defined in (13) to compare this work with the state of the art

$$\rm FOM_2 = 10\log\left(\frac{IMFDR_{gm,lin}\times f_{-3dB,gm}\times Tuning}{ppp_{gm}}\right) \quad (13)$$

where $\rm IMFDR_{gm,lin}$ is the IMFDR calculated using $(2/3)(\rm IIP3 - \mathit{N})$ and here expressed as a ratio (no unit). The subscript gm, lin implies geometrical mean as the value has been averaged for low- and high-frequency BWs in the linear scale. IIP3 is the input third-order intercept point (in dBm), and N is the IRN spectral density (in dBm per hertz). $f_{-3\rm dB,gm}$ is the cutoff frequency geometrical mean (in hertz). Tuning is the ratio $f_{-3\rm dB,max}/f_{-3\rm dB,min}$ (no unit). $\rm ppp_{gm}$ is the power geometrical mean per pole quantity (in watts). This work measures better $\rm FOM_1$ and $\rm FOM_2$. Due to the parasitic limits of the employed 0.18-μm CMOS process, the achieved $f_{-3\rm dB}$ is not as high as that in [3], but the measured $f_{-3\rm dB}$ tunability is at least $11.75\times$ beyond them, also owing to the use of an elevated $V_{\rm DD}$.

V. CONCLUSION

We have successfully demonstrated a current-reuse SFAI that can effectively transform a *first-order SF-based LPF* into a *third-order transistorized-LC-ladder LPF*. Specifically, with an increased $V_{\rm DD}$ to 3 V, an SF, an SFAI, and a feedforward capacitor together can implement a Chebychev-II response in one branch with extensive BW–power scalability. The fabricated LPF prototype not only shows a very high area efficiency (0.0046 $\rm mm^2$ per pole) but also measures better figures of merit compared with those of the state of the art.

ACKNOWLEDGMENT

The authors would like to thank Z. Ye, L. Zhang, and J. Yang for their help and Agilent OpenLAB for test support.

REFERENCES

[1] M. S. Oskooei, N. Masoumi, M. Kamarei, and H. Sjöland, "A CMOS 4.35-mW + 22-dBm IIP3 continuously tunable channel select filter for WLAN/WiMAX receivers," *IEEE J. Solid-State Circuits*, vol. 46, no. 6, pp. 1382–1391, Jun. 2011.

[2] K. Kwon and K. Lee, "A 23.4 mW 68 dB dynamic range low band CMOS hybrid tracking filter for ATSC digital TV tuner adopting RC and Gm-C topology," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 10, pp. 2346–2354, Oct. 2011.

[3] F. Houfaf, M. Egot, A. Kaiser, A. Cathelin, and B. Nauta, "A 65 nm CMOS 1-to-10 GHz tunable continuous time low-pass filter for high-data-rate communications," in *Proc. IEEE ISSCC Tech. Dig.*, Feb. 2012, pp. 362–363.

[4] A. Tajalli and Y. Leblebici, "Low-power and widely tunable linearized biquadratic low-pass transconductor-C filter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 3, pp. 159–163, Mar. 2011.

[5] T. Lo, C. Hung, and M. Ismail, "A wide tuning range $\rm G_m - C$ filter for multi-mode CMOS direct-conversion wireless receivers," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2515–2524, Sep. 2009.

[6] T. Lo and C. Hung, "A wide tuning range Gm-C continuous-time analog filter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 4, pp. 713–722, Apr. 2007.

[7] D. Chamla, A. Kaiser, A. Cathelin, and D. Belot, "A $\rm G_m - C$ low-pass filter for zero-IF mobile applications with a very wide tuning range," *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1443–1450, Jul. 2005.

[8] S. D'Amico, M. Conta, and A. Baschirotto, "A 4.1-mW 10-MHz fourth-order source-follower-based continuous-time filter with 79-dB DR," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2713–2719, Dec. 2006.

[9] A. Pirola, A. Liscidini, and R. Castello, "Current-mode, WCDMA channel filter with in-band noise shaping," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1770–1780, Sep. 2010.

[10] P.-I. Mak and R. P. Martins, "High-/mixed-voltage RF and analog CMOS circuits come of age," *IEEE Circuits Syst. Mag.*, vol. 10, no. 4, pp. 27–39, 4th Quart., 2010.

[11] D. E. Bockelman and W. R. Eisenstadt, "Combined differential and common-mode scattering parameters: Theory and simulation," *IEEE Trans. Microw. Theory Tech.*, vol. 43, no. 7, pp. 1530–1539, Jul. 1995.