Self-tracking charge pump for fast-locking PLL

Y. Chen, P.-I. Mak and Y. Zhou

Presented is a self-tracking charge pump (ST-CP) that can deliver a non-constant current over the output voltage range for a fast-locking phase-locked loop (PLL). It features a simple self-bias self-tracking architecture that can reduce, simultaneously, the PLL locking time and the current mismatch in charge and discharge phases. Experimentally verified in a 0.18 μm CMOS process, the proposed ST-CP achieves 72% reduction of PLL locking time compared with the conventional one. The core occupies 30 × 60 μm^2 and draws 10 μA at 1.8 V.

Introduction: Phase-locked loops (PLLs) have been widely utilised in high-speed data transmission systems such as wireless transceivers, disk read/write channels and high-speed interfaces. In these applications, the PLLs are required to feature low phase noise and fast-locking time which are linked with the loop bandwidth of the PLL. A wide loop bandwidth shorts the locking time, whereas a narrow loop bandwidth reduces the phase noise of the locked oscillator. Several adaptive bandwidth methods have been developed to achieve a loose tradeoff between the phase noise and locking time. These methods unavoidably call for extra circuitry such as adaptive bandwidth controller [1], discriminator-aided phase detector with a modified loop filter [2] and modulated bias current source [3].

In this Letter, a self-tracking charge pump (ST-CP) that can speed up the PLL locking time while balancing the charge and discharge currents with simple hardware is proposed.

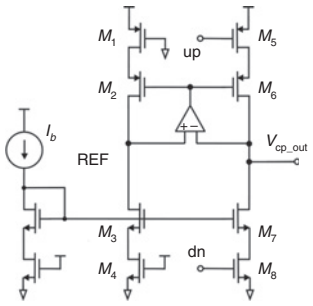

Fig. 1 *Conventional CP*

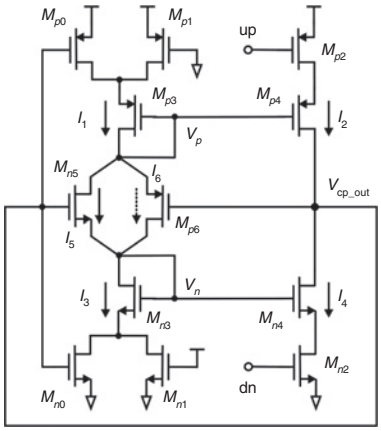

Fig. 2 *Proposed ST-CP*

Conventional and proposed CPs: Fig. 1 shows a typical charge pump (CP) [4] that has been widely employed for its low bias current, high deliverable output current and reasonable switching time. However, in order to stabilise the output current over the output voltage range, a negative feedback amplifier is entailed. As long as the amplifier can offer a high enough gain the voltage at the node REF of the current generator (M_1–M_4) will follow the voltage at the node V_{cp_out} of the charge pump core (M_5–M_8). In this way, a well-matched charge-discharge current can be achieved, at the expense of extra power and hardware.

Differently, the proposed ST-CP exploits a feedback control cell. It consists of PMOS (M_{p6}) and NMOS (M_{n5}) to dynamically trace the non-constant charge/discharge current as shown in Fig. 2. It features a simpler architecture than the conventional one as the negative feedback amplifier is no longer necessary. The operation of the circuit is described as follows: first, the channel-length modulation effect is ignored for simplicity. M_{n3} and M_{n4} are of equal size. If V_{cp_out} is higher than half of the supply voltage (V_{dd}), the feedback transistor M_{p6} will be turned off while M_{n5} will be on. If the 'up' and 'dn' signals are of high level, the current relationship is $I_1 = I_5 = I_3 = I_4$. I_3 and I_5 can be given as

$$I_3 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{Mn3}(V_{GS\_Mn3} - V_{th\_Mn3})^2 \quad (1)$$

$$I_5 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{Mn5}(V_{GS\_Mn5} - V_{th\_Mn5})^2 \quad (2)$$

where $V_{GS\_Mn5} = V_{cp\_out} - V_n$, $V_{GS\_Mn3} = V_n$. V_{th} is the threshold voltage, $\mu_n C_{ox}$ and W/L are transistor parameters and size aspect ratio, respectively. The relation of V_{cp_out} and V_n can be derived from (1) and (2) as given by

$$V_n = \frac{k}{1+k}V_{cp\_out} - \frac{kV_{th\_Mn5} - V_{th\_Mn3}}{1+k} \quad (3)$$

where $k = \sqrt{(W/L)_{Mn5}/(W/L)_{Mn3}}$ and V_n is proportional to V_{cp_out}. I_4 can be given by

$$\begin{aligned} I_4 &= \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{Mn4}(V_{GS\_Mn4} - V_{th\_Mn4})^2 \\ &= \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{Mn4} \\ &\quad \times \left(\frac{k}{1+k}V_{cp\_out} - \frac{kV_{th\_Mn5} - V_{th\_Mn3}}{1+k} - V_{th\_Mn4}\right)^2 \end{aligned} \quad (4)$$

where $V_{GS\_Mn4} = V_{GS\_Mn3} = V_n$. The relation between the discharge current and the output voltage of the CP satisfies the square law, similar to I_{ds} against V_{gs} of an MOS transistor in the saturation region.

An increment of the CP output voltage also increases the discharge current. Similarly, M_{p3} and M_{p4} are of equal size. If the V_{cp_out} is lower than half of the V_{dd}, the feedback transistor M_{n5} will be turned off while M_{p6} will be on. If the 'up' and 'dn' signals are of low level, the current relationship becomes $I_1 = I_6 = I_3 = I_2$. The relationship between the charge current and the output voltage of the CP also satisfies the square law. The charge current will be increased when the output voltage of the CP decreases. The charge current I_2 can be made equal to the discharge current I_4 owing to the following feedback mechanism: if V_{cp_out} increases from a lower value to $V_{dd}/2$, M_{p6} will be activated in the feedback control cell. V_p follows V_{cp_out} owing to the source follower M_{p6}. The current in the current generator decreases according to the path: $I_1 \rightarrow I_6 \rightarrow I_3$, resulting in a parallel decrement of the charge and discharge currents (I_2 and I_4). An analogue mechanism exists when V_{cp_out} increases from $V_{dd}/2$ to a higher value, leading to a parallel increment of the charge and discharge currents. Additionally, the ST-CP implements the current variation (high-to-low-to-high) when the output voltage changes from low to high.

In practice, the channel-length modulation effect can influence the current unbalance between the charge and discharge current mirrors. Two feedback transistors, M_{n0} and M_{p0}, are added to compensate for this effect [5].

Fig. 3 shows the simulated charge/discharge current as the CP output voltage sweeps from 0 to 1.8 V. The output dynamic voltage range of the two CPs is from 0.3 to 1.5 V. The conventional CP maintains the charge/discharge currents constant across the CP output dynamic voltage range. Differently, for the ST-CP, the relation between the current (I_{cp}) and the output voltage (V_{cp_out}) of the ST-CP satisfies the square law, and can be expressed as

$$I_{cp} \propto A(V_{cp\_out} - B)^2 \quad (5)$$

where A and B are constant variables. The charge/discharge current decreases as the ST-CP output voltage increases from 0.3 to 0.9 V (low $V_{dd}/2$ region), and the charge/discharge current increases as the ST-CP output voltage increases from 0.9 to 1.4 V (high $V_{dd}/2$ region). This demonstrates that the charge/discharge current is dynamic over the CP output voltage range.

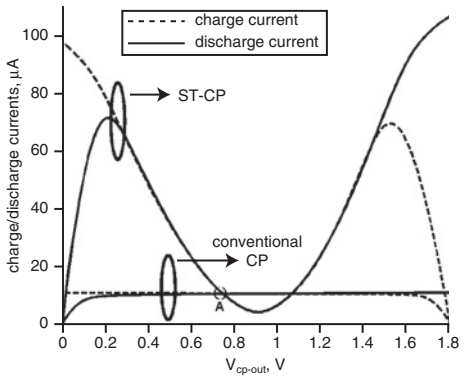

Fig. 3 *Charge/discharge currents of conventional CP and proposed ST-CP*

Experimental results and discussion: Two narrowband 1 GHz PLLs with the conventional CP and proposed ST-CP were fabricated in a 0.18 μm CMOS process. The die photograph is shown in Fig. 4. The die area of the ST-CP is about 30 × 60 μm^2. When the PLL is in locking state, the ST-CP consumes (average) 10 μA at 1.8 V.

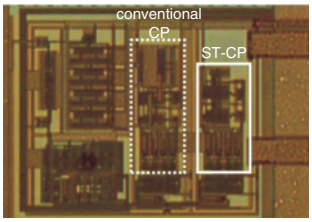

Fig. 4 *Die photograph*

For a type-II, third-order PLL, the crossover frequency can be approximated as

$$\omega = \frac{I_{cp} K_{VCO} R_z}{2\pi N} \quad (6)$$

where I_{cp} is the charge pump current, K_{VCO} is the VCO sensitivity, R_Z is the loop filter resistor, N is the integer division ratio. According to (6), ω is the loop bandwidth and is directly proportional to I_{cp} when other parameters are fixed. During the output dynamic voltage range of the CP, the charge/discharge current dynamically changes with the corresponding loop bandwidth. The point 'A' in Fig. 3 is the desired locking point which is also the current cross-point between the conventional CP and proposed ST-CP. Thus, the same loop parameters can be achieved to compare, fairly, the locking time of the proposed ST-CP with that of the conventional one. During the out-of-lock state, the loop bandwidth ω of the PLL with the ST-CP is wider than that of the PLL with the conventional CP, owing to the larger I_{cp} in the ST-CP. Therefore, a fast acquisition time is achieved. Meanwhile, as the PLL moves toward the locking state, the loop bandwidth is reduced with I_{cp} decreasing in order to implement a narrow bandwidth, so that the acquisition speed is gradually decreased. Once the desired operating frequency is locked, the PLL will maintain the same and narrow loop bandwidth to suppress the phase noise. Thus, the locking time of the PLL is reduced more effectively by using the proposed ST-CP.

Figs. 5*a* and *b* show the measured PLL control-voltage waveforms of the locked oscillator with the conventional CP and proposed ST-CP, respectively. The PLL locking time is 5 μs with the conventional CP, but is shortened to 1.4 μs (72% reduction) with the proposed ST-CP.

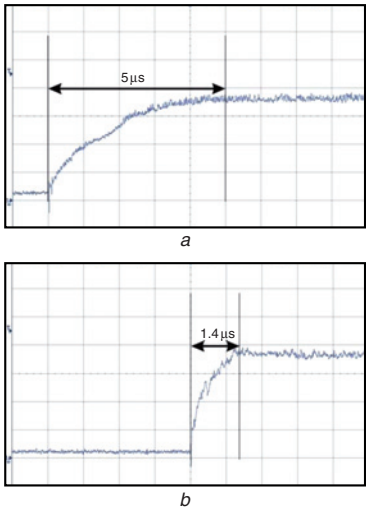

Fig. 5 *Measured PLL locking time*

a Conventional CP
b Proposed ST-CP

Conclusion: An ST-CP that can dynamically trace the charge/discharge current over the output voltage range is proposed and experimentally verified. It features simple self-bias self-tracking architecture and matched charge and discharge currents. It can effectively speed up the PLL locking time by 72% when compared with the conventional one.

4 January 2010
doi: 10.1049/el.2010.3562
One or more of the Figures in this Letter are available in colour online.

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