A 0.07 mm^2 2.2 mW 10 GHz Current-Reuse Class-B/C Hybrid VCO Achieving 196-dBc/Hz FoM$_A$

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***Abstract*—This Letter describes a current-reuse class-B/C hybrid voltage-controlled oscillator (VCO) with robust startup, enhanced phase noise and differential balancing at small area and power. Specifically, an asymmetrical CMOS class-C core is aided by a symmetrical NMOS-only class-B core that effectively shares the bias current for deeper class-C operation of the former; wider margin of startup against PVT variations, and lower amplitude imbalance against oscillation frequencies. Moreover, this topology adds the freedom of adjustable peak dynamic current and boosts the oscillation swing at low power. The spiral inductors with patterned ground shields shrink the die size. Fabricated in 65 nm CMOS, the 0.07 mm^2 VCO prototype exhibits 10.15-to-11.17 GHz tunability, and -107.73-dBc/Hz phase noise at 1 MHz offset, while dissipating merely 2.2 mW at 1.2 V. The achieved area-included figure-of-merit (FoM$_A$ = 196 dBc/Hz) favorably compares with the state-of-the-art.**

***Index Terms*—Current-reuse, CMOS, class-B, class-C, phase noise, startup, voltage-controlled oscillator (VCO).**

I. Introduction

VOLTAGE controlled oscillator (VCO) is still one of the most area-and-power-hungry blocks of nanoscale CMOS wireless transceivers. In fact, it is challenging to realize an ultra-compact VCO while still keeping state-of-the-art phase noise and power consumption, as a small inductor intrinsically results in lower LC tank's impedance that in return demands a larger bias current to secure an adequate output swing [1].

Compared with the conventional class-B LC-VCOs using an NMOS-/PMOS-only cross-coupled pair, the CMOS current-reuse class-B VCO [Fig. 1(a)] can halve the bias current while offering the same negative transconductance and output swing, being an attractive approach to save the power [2]. Yet, CMOS current-reuse VCO is architecturally asymmetrical, rendering its differential balancing sensitive to the peak dynamic current in the period when both M_1 and M_2 are switched on. Thus, extra source or drain resistors [2], [3], or cascaded PMOS and NMOS transistors [4], [5], are required to limit the peak dynamic current in order to prevent M_1 and M_2 from entering into the deep triode region. To eliminate those extra components while reducing the power, [6] reported a CMOS current-reuse class-C VCO with an adaptive bias scheme [Fig. 1(b)] to aid the startup and output differential balancing through an undistorted dynamic current. Good balancing was only demonstrated over a narrow frequency tuning range (FTR) of 2.2%.

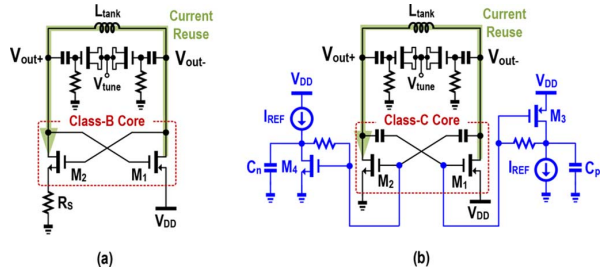

Fig. 1. Current-reuse VCO: (a) class-B [2] and (b) class-C with an adaptive bias scheme [6].

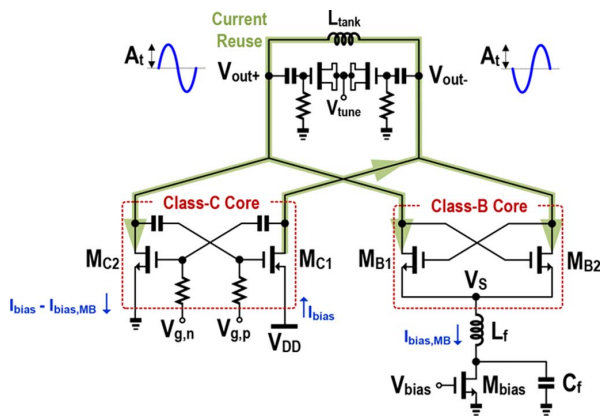

Fig. 2. Proposed current-reuse class-B/C hybrid VCO.

This Letter proposes a current-reuse class-B/C hybrid VCO as shown in Fig. 2. Besides to ensure the startup of the class-C core by adding a class-B cross-coupled pair [7], this design also features: 1) a CMOS current-reuse class-C core to reduce the power consumption while still maintaining a good phase noise, and 2) improved balancing of the differential outputs over a reasonably wide FTR with the help of a balanced class-B cross- coupled pair. Interactively, the class-B cross-coupled pair also facilitates the class-C core to operate in the current-limited

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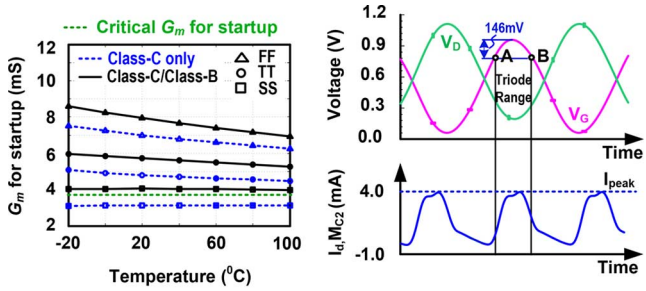

Fig. 3. Simulated (a) small signal G_m versus temperature at different process corners (SS, TT, FF), and (b) transient waveforms of the gate and drain voltages and drain current of M_{C2}.

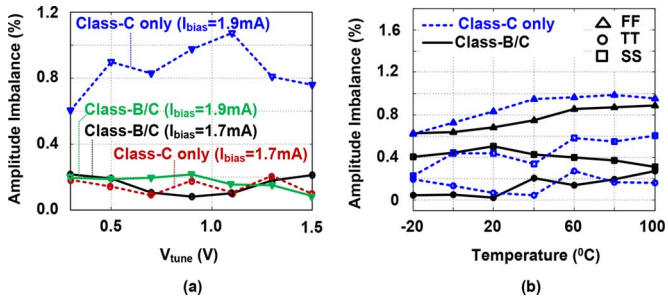

Fig. 4. Simulated amplitude imbalance of the class-C only and class-B/C VCOs against (a) $V_{\rm tune}$ and (b) temperature at different process corners.

region, resulting in a larger output swing that further reduces phase noise.

II. Proposed Current-Reuse Class-B/C Hybrid VCO

For a class-B/C hybrid VCO, the steady-state performance is dominated by the class-C core that should consume most of the bias current. Thus, current-reuse is particularly effective for the class-C core. Recalling Fig. 2, the CMOS transconductor $M_{\rm C1}$ ($g_{\rm mc1}$, 40/0.06 μm) and $M_{\rm C2}$ ($g_{\rm mc2}$, 14/0.06 μm) should be asymmetrical in dimensions to counteract their differences in process parameters. Ideally, the gate bias $V_{\rm g,p}$ and $V_{\rm g,n}$ have to be set lower than the device's threshold voltage for deeper class-C operation. This act however leads to a small negative transconductance worsening the startup robustness (i.e., failed to oscillate against PVT variations and long startup time). As a result, by paralleling the asymmetrical class-C with a symmetrical class-B using an NMOS-only cross-coupled pair ($M_{\rm B1}$ and $M_{\rm B2}$ with $g_{\rm mB}$), the effective negative transconductance $(-G_{\rm m})$ can be balanced better and boosted to $-G_m = -(g_{mc1} \| g_{mc2} + g_{mB}/2)$ for robust startup.

The primary concern of a current-reuse VCO is to operate it in the current-limited region as the voltage-limited region will directly result in asymmetrical differential outputs. Moreover, in the voltage-limited region, the device's conduction angle is wider, penalizing the DC-to-RF current-conversion efficiency. In the current-limited region, $V_{\rm g,n}$ and $V_{\rm g,p}$ have to be chosen such that both $M_{\rm C1}$ and $M_{\rm C2}$ remain in saturation. The maximum single-ended oscillation amplitude $(A_{\rm t})$ is thus limited by (assuming the same common voltage): $A_t < (V_{g,p} - V_{g,n} + |V_{th,p}| + V_{th,n})/4$, where $V_{\rm th,p}(V_{\rm th,n})$ denotes the threshold voltage of $M_{\rm C1}(M_{\rm C2})$. $A_{\rm t}$ can be maximized by increasing the voltage difference between $V_{\rm g,p}$ and $V_{\rm g,n}$. Yet, when considering the differential balancing, $V_{\rm g,p}$ and $V_{\rm g,n}$ should be chosen for an equal transconductance of $M_{\rm C1}$ and $M_{\rm C2}$. Here, with the design freedom provided by the class-B core, $V_{\rm g,n}$ can be reduced comfortably for differential balancing, while boosting the oscillation swing for better phase noise.

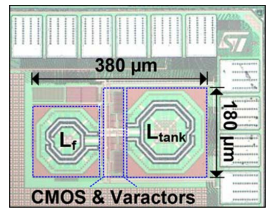

Fig. 5. Chip photo of the proposed VCO fabricated in 65 nm CMOS.

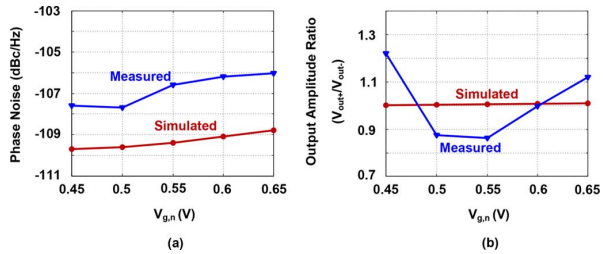

Fig. 6. Simulated and measured (a) phase noise, and (b) amplitude ratio as a function of $V_{\rm g,n}$ when $V_{\rm g,p}$ is fixed at 0.6 V.

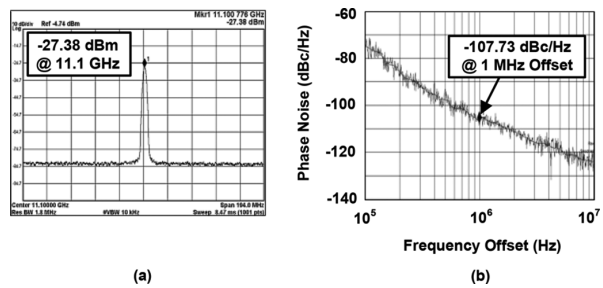

Fig. 7. Measured (a) output spectrum and (b) phase noise.

The theoretical output amplitude of the current-reuse class-B/C VCO is $[(2/\pi)I_{\rm bias,MB} + (I_{\rm bias} - I_{\rm bias,MB}) + I_{\rm bias}]R_P$, where $R_{\rm p}$ is the parallel resistance of the LC tank, $I_{\rm bias}$ is the total bias current and $I_{\rm bias,MB}$ is the bias current diverted into $M_{\rm B1,2}$ (10/0.06 μm). Since the current efficiency of the class-B core is only 63.7% of that of the class-C core [7], the choice of $I_{\rm bias,MB}$ is a trade-off between the power efficiency and robust startup. In this design, $I_{\rm bias,MB}$ is chosen as 30% of $I_{\rm bias}$ for reliable startup against PVT variations. Fig. 3(a) shows the simulated small-signal G_m at different process corners (SS, TT, FF) and over a wide range of temperature (-20 to 100°C) for both the class-C-only VCO and the current-reuse class-B/C VCO under the same bias current. The critical G_m for startup (3.6 mS) is marked. Thanks to the added class-B core, the current-reuse class-B/C VCO can safely meet the startup conditions for process corners and temperature, while the class- C only VCO fails to startup at the SS corner.

The transient waveforms of the gate and drain voltages and drain current of $M_{\rm C2}$ are plotted in Fig. 3(b). When carrying the maximum current, the NMOS is slightly pushed out of the saturation region with a maximum $V_{gs} - V_{th,n} - V_{ds} = 0.146$ V. Yet, the transient current waveforms are still effectively in class-C for all operational current levels.

For the class-B core, in order to reduce the phase noise introduced by the tail transistor $M_{\rm bias}$, it is upsized appropriately to minimize its flicker noise. Furthermore, the inductor L_f is employed to resonate with C_f at twice the VCO oscillation frequency $(f_{\rm osc})$ as shown in Fig. 2. From simulations, a very small

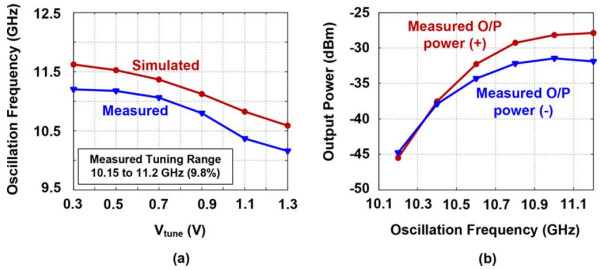

Fig. 8. (a) Simulated and measured FTR. (b) Measured output powers.

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART

	[1] MWCL'07	[4] MWCL'08	[6] RFIC'13	[9] ASSCC'12	This Work
Technology	180 nm	180 nm	180 nm	65 nm	**65 nm**
Topology	Current-Reuse	Current-Reuse	Class-C Current-Reuse	Ac-coupled Current-Reuse	**Class-B/C Current-Reuse**
f_{osc} (GHz)	2.4	16	4.6	2.53	**11.2**
FTR (%)	13.7	5.6	2.2	29	**9.6**
Power (mW)	0.97	8.1	2.4	0.28	**2.2**
PN @ 1 MHz (dBc/Hz)	-111	-111	-118 #	-112 #	**-107.73**
Die Area (mm^2)	0.47*	0.15*	0.18	0.13	**0.07**
FoM [1] (dBc/Hz)	179	187	187	185	**185**
FoM$_A$ [2] (dBc/Hz)	182	195	194	194	**196**
FoM$_T$ [3] (dBc/Hz)	182	181	174	194	**185**

Normalized from original measured data * Estimated core area

[1] $\text{FoM} = 10\log_{10}\left(\left(\frac{f_{osc}}{\Delta f}\right)^2 \frac{1}{P_{diss}(mW)}\right) - \text{PN}$

[2] $\text{FoM}_A = \text{FoM}^{[1]} - 10\log_{10}[\text{Area}(\text{mm}^2)]$, [3] $\text{FoM}_T = \text{FoM}^{[1]} - 20\log_{10}\left[\frac{\text{FTR}}{10}\right]$

inductance of 0.4 nH is adequate to reduce the phase noise by 7 dB (3 dB) at 10 kHz (1 MHz) offset.

Fig. 4(a) plots the simulated amplitude imbalance against the frequency tuning voltage (V_{tune}) at different bias currents, which are set by changing $V_{\text{g,p}}$ and $V_{\text{g,n}}$. For a lower bias current of 1.7 mA, the amplitude imbalance for both class-C only and class- B/C VCOs are $< 0.22\%$. However, when the bias current goes up to 1.9 mA, the amplitude imbalance for the class-B/C VCO is still kept the same, while that for the class-C only VCO is degraded to 1.1%. Transistor and capacitor mismatches also can affect the differential balancing. At $I_{\text{bias}} = 1.7$ mA and $V_{\text{tune}} = 0.3$ (1.2) V, Monte Carlo simulations show that the mean of amplitude imbalance is 0.14% (0.7%) for the class-B/C VCO, and 1.6% (1.4%) for the class-C only VCO. Fig. 4(b) gives the simulated amplitude imbalance over temperature at 3 process corners. The worst amplitude imbalance for the class-B/C VCO is 0.9% at 100°C, under the FF process corner. This shows that class-B/C VCO has robust differential balancing against frequency, bias and process variations.

III. MEASUREMENT RESULTS

The proposed VCO targets a 10 GHz f_{osc} and ~10% FTR. It was fabricated in a standard ST 65 nm CMOS process without any ultra-thick metals. The die area of the *LC* tank is minimized by choosing a small inductor of 0.8 nH with a patterned ground shield, which has a simulated Q of ~5. Fig. 5 shows the chip photo of the VCO occupying a small die size of 380 $\times$ 180 μm^2. During the measurements, $V_{\text{g,n}}$ and $V_{\text{g,p}}$ are kept constant when the VCO starts up. Fig. 6 depicts the measured phase noise and amplitude ratio versus $V_{\text{g,n}}$ when $V_{\text{g,p}}$ is fixed at 0.6 V. It can be seen that $V_{\text{g,n}} = 0.5$ V allows the low phase noise at low power consumption with a reliable startup, even with a sub-optimum amplitude imbalance ratio. Thus, $V_{\text{g,n}}$ and $V_{\text{g,p}}$ are set at 0.5 and 0.6 V, respectively, for other measurements. The VCO consumes 2.2 mW at a 1.2 V supply. At 11.1 GHz, the measured output power is -27.38 dBm as shown in Fig. 7(a) via an open-drain test buffer. The phase noise at 1 and 10 MHz offsets are -107.73 and -123 dBc/Hz, respectively, as depicted in Fig. 7(b). The FTR is from 10.15 to 11.17 GHz (9.6%) when V_{tune} changes from 0.3 to 1.2 V as shown in Fig. 8(a). Fig. 8(b) shows the measured output power at the two differential output terminals as a function of V_{tune}. The power discrepancy at higher frequency should be due to the impedance mismatch of the bondwire and PCB traces (consistent with ~10% mismatch in their parasitic capacitances, from simulations). For more accurate measurements of the amplitude imbalance, a better EM model and on-chip downconversion mixer might be added to downconvert the signal to low frequency first, such that the effect of mismatch at the output ports can be minimized [8]. Table I summarizes the results and compares this work with the relevant art using current-reuse and class-C techniques [1], [4], [6], [9]. This work attains comparable figure-of-merits (FoMs), particularly the area-included FoM$_A$ of 196 dBc/Hz.

IV. CONCLUSION

This Letter reported a 65 nm CMOS 10 GHz current-reuse class-B/C hybrid VCO achieving a state-of-the-art performance in a small die area of 0.07 mm^2. The key technique is to parallel an asymmetrical current-reuse class-C core with a symmetrical class-B core that effectively shares the bias current for a deeper class-C operation of the former, while improving the startup condition, differential balancing and oscillation swing. The achieved phase noise is -107.73 dBc/Hz at 1 MHz offset while drawing only 2.2 mW at 1.2 V. The achieved FoM, FoM$_A$ and FoM$_T$ are 185, 196 and 185 dBc/Hz, respectively.

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