0.45-V 5.4-nW switched-capacitor bandgap reference with intermittent operation and improved supply immunity

Ziyang Luo, Yan Lu✉ and Rui P. Martins

Switched-capacitor networks have been used as bandgap references (BGRs) to replace the area-consuming resistors in ultra-low power applications, incorporated with voltage doubler (2X) charge pumps to operate at low supply voltages. However, the open-loop charge pumps are sensitive to supply and load variations. Therefore, in this work, constant bias currents are added to the cross-coupled 2X charge pumps to reduce the supply sensitivity, and also to reduce the output ripples without using large capacitors. To further reduce the power consumption, a low-leakage sample and hold (S&H) circuit is used for an intermittent operation, the active/idle duty ratio of the BGR core is 1/15. Designed in standard 65 nm CMOS, the proposed BGR reaches a temperature coefficient of 64 ppm/°C consuming only 5.4 nW with a minimum supply of 0.45 V (simulated).

Introduction: Low power and low supply circuits have drawn increasing attention in recent years [1–3], due to the blooming internet-of-things. For bandgap references (BGRs), the resistors which determine the BGR current consumption limit the area and power trade-off. From [1], a switched-capacitor network (SCN) including two single-branch 2X charge pumps removes the resistors and allows operation at the low supply voltage. However, the open-loop charge pump makes the BGR sensitive to supply variations, because the ratio of the equivalent currents delivered to the two bipolar junction transistor (BJT) branches changes with supply voltage. Also, the single-branch charge pump has relatively large output ripples. In [2], a sample and hold circuit is used for an intermittent operation to achieve an ultra-low power consumption of 2.98 nW. However, it forces a continuous-time BGR core into discontinuous operation. Besides, its supply voltage is high and the resistors occupy a large chip area. Since both the above-mentioned techniques involve the discrete-time operation, it is natural to combine them for an ultra-low power, low voltage, and small area solution. Moreover, the supply sensitivity issue should be addressed.

In this Letter, we propose a switched-capacitor BGR with intermittent operation using a cross-coupled 2X charge pump with a constant-current bias to reduce the supply voltage sensitivity and output ripple. Besides, we design a 1/4 ratio voltage divider in the SCN for a lower output reference voltage, which consumes less power because there is no direct discharge to the ground for all the capacitors.

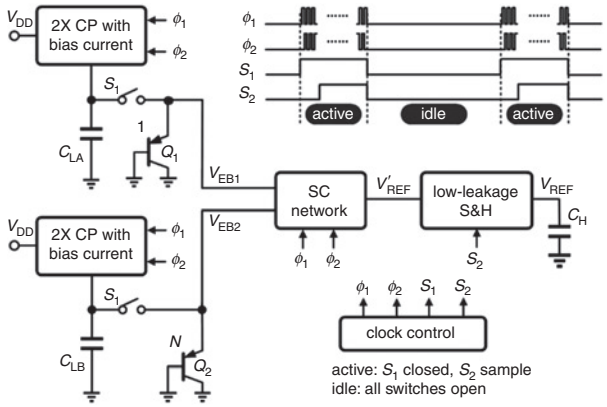

Fig. 1 *Architecture of the proposed BGR*

Circuit implementation: Fig. 1 shows the architecture of the proposed BGR. When the BGR operates in the active mode ($S_1 = 1$), the cross-coupled 2X charge pumps with added bias current I_{BIAS}, as shown in Fig. 2, provide the same bias current to the BJTs Q_1 and Q_2 while reducing the minimum supply voltage down to 0.45 V. In this work, the cross-coupled charge pump generates less ripple, when compared to the single-branch charge pump used in [1]. The SCN divides V_{EB2} by 4 and sums up $V_{EB2}/4$ and the proportional-to-absolute-temperature voltage ΔV_{EB}, where $\Delta V_{EB} = V_T \times \ln(N)$, to generate the reference voltage V'_{REF}. Then, C_H stores V'_{REF} as V_{REF} through the low-leakage sample and hold circuit [4]. When the BGR operates in the idle mode ($S_1 = 0$), all the switches in the cross-coupled 2X charge pump and the SCN turn off for power saving. When the BGR core wakes up, the charge stored on the capacitors C_{LA} and C_{LB} speeds up the process of V_{EB1} and V_{EB2} recovering to their normal voltages.

Fig. 3 shows the SCN of the BGR core. In the active mode, there are two phases ϕ_1 and ϕ_2 to control the SCN. In ϕ_1, four capacitors (C_{M1-4}) in series connect to V_{EB2}, while the voltage across the two capacitors C_{N1} and C_{N2}, in parallel, is ΔV_{EB}. In ϕ_2, C_{M1-4} are in parallel thus their voltage is $V_{EB2}/4$; C_{N1} and C_{N2} in series generate $2\Delta V_{EB}$. Therefore, the generated reference voltage V'_{REF} in ϕ_2 will become

$$V'_{REF} = 2V_T \ln(N) + V_{EB2}/4 \approx 300\,\text{mV}. \quad (1)$$

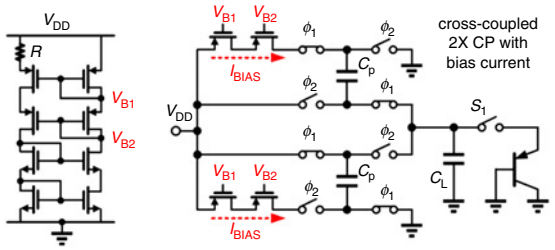

Fig. 2 *Cross-coupled voltage doubler with a bias current*

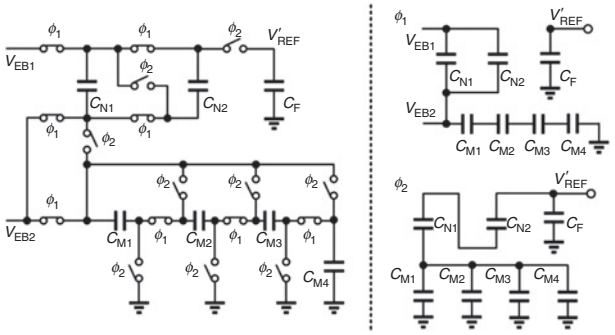

Fig. 3 *SCN for obtaining V'_{REF}*

As mentioned above, this SCN consumes less power than the SCN in [1] because there is no capacitor being discharged to the ground.

Fig. 4 exhibits the clock control unit. The current source shown in Fig. 2 provides bias currents (about 1.25 nA at room temperature) for the current starving ring oscillator composed of three inverters. The generated frequency is close to 50 kHz with 0.45 V supply voltage at room temperature. Considering the trade-off between the output ripple and the power consumption, we choose 12 D-flip-flops as a frequency divider and the BGR active/idle duty ratio is 1/15. To step-up the non-overlapping and the duty-cycle control signals, we employ a separate 2X charge pump, with energy-efficient level shifters [5].

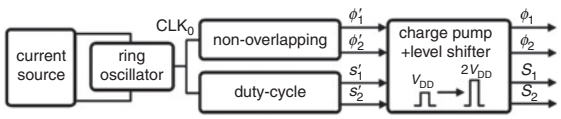

Fig. 4 *Block diagram of the clock control unit*

Fig. 5 shows the low-leakage sample and hold circuit, which consumes a tiny power value (0.4 nW). In the active mode, as shown in the timing diagram of Fig. 1, there is a gap period between $S_1 = 1$ and $S_2 = 1$, because the BGR core needs some time to recover to proper operation. In the idle mode, the unity-gain buffer works as a follower to reduce the V_{DS} and V_{BS} of M_{H2}, therefore, it results in very low leakage currents. To reduce the channel injection and clock feedthrough effects, we choose the minimum size for the switches M_{H1}, M_{H2} and M_{H3}. Besides, we use MIM capacitors, 16 pF in total, for the flying capacitors to reduce the parasitic capacitance. We also utilise thick-oxide MOS capacitors, 75 pF in total, for C_{LA}, C_{LB}, C_F, and C_H, to reduce the output ripple with a small area.

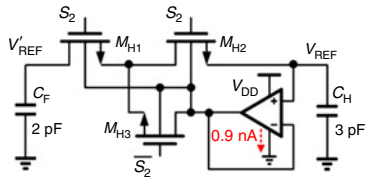

Fig. 5 *Low-leakage sample and hold circuit*

Simulation results: Fig. 6 shows the simulated results of reference voltage V_{REF} as a function of temperature at different supply voltages with/without the bias current in the cross-coupled 2X charge pump. The simulated temperature coefficient (TC) is 64 ppm/°C at 0.45 V supply and 16 ppm/°C at 0.5 V supply with bias current. As the supply voltage changes from 0.45 to 0.6 V, the proposed BGR shows a line sensitivity of 1.5%/V, while it is 13.8%/V without bias current. Fig. 7 displays the total power consumption from 0 to 80°C with different supply voltages. The power consumption at room temperature with 0.45 V supply is close to 5.4 nW. Fig. 8 illustrates the reference voltage V_{REF} as a function of temperature in different corners. The result shows the worst-case TC is 104 ppm/°C in ff corner because V_{EB2} increases with larger bias currents at high temperature. Fig. 9 plots the start-up curve of the generated V_{REF}, with steady-state ripples of 16 µV. Table 1 presents the performance comparison with state-of-the-art works. The proposed work exhibits the lowest supply voltage and the smallest output ripple without using large capacitor values. Comparing with [1], this work consumes less power and is less sensitive to supply variations.

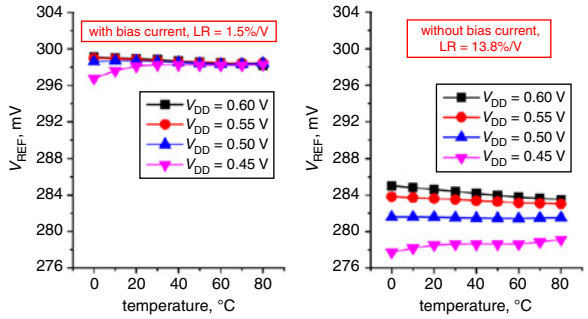

Fig. 6 *V_{REF} at different supply voltages with or without the bias current*

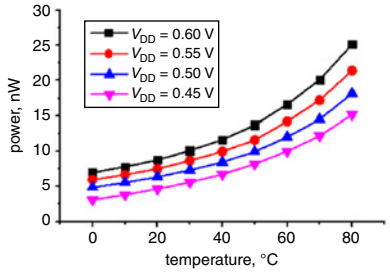

Fig. 7 *Power consumption of the BGR at different supply voltages*

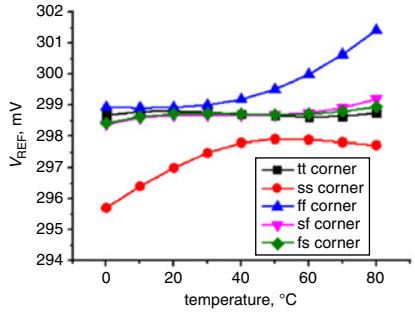

Fig. 8 *Simulated BGR V_{REF} in tt, ff, ss, sf and fs corners*

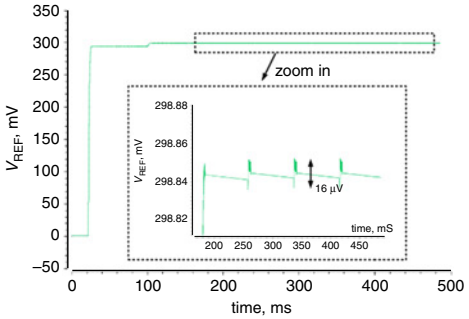

Fig. 9 *Start-up curve of the BGR and its output ripple*

Table 1: Performance comparison with state-of-the-art BGRs

	[1]	[2]	[4]	This work
Technology	0.13 µm	0.18 µm	0.18 µm	65 nm
V_{REF} (V)	0.5	1.2	0.256	0.3
Min. V_{DD} (V)	0.5	1.4[a]	0.75	0.45
Power	32 nW	2.98 nW	170 nW	5.4 nW
TC (ppm/°C)	75	24.74	40	64
Line reg. (%/V)	NA	0.062	NA	1.5
Ripple	50 µV	100 µV	20 mV	16 µV

[a]Estimated from the figure.

Conclusion: This Letter proposed an ultra-low power and low supply BGR circuit, generating a reference voltage of 300 mV (1/4 of the bandgap voltage) with a typical TC of 64 ppm/°C. By using a cross-coupled 2X charge pump with a bias current to enable the BGR to operate as low as 0.45 V supply, we improved both the supply immunity and the output ripple. With the intermittent operation, the BGR consumes an ultra-low power of 5.4 nW.

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One or more of the Figures in this Letter are available in colour online.

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