A 3.8mW 8b 1GS/s 2b/cycle Interleaving SAR ADC with Compact DAC Structure

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Abstract

An 8b 1GS/s ADC is presented that interleaves two 2b/cycle SARs. To enhance speed and save power, the prototype utilizes segmentation switching and custom-designed DAC array with high density in a low parasitic layout structure. It operates at 1GS/s from 1V supply without interleaving calibration and consumes 3.8mW of power, exhibiting a FoM of 24fJ/conversion step. The ADC occupies an active area of 0.013mm^2 in 65nm CMOS including on-chip offset calibration.

Introduction

Medium resolution GHz sampling rate low power ADC is in high demand for next generation communication systems. While sub-ranging flash and folding pipeline architectures enable the implementation over GS/s with 7~8b resolution, their reported energy per conversion step (FoM) is no less than 100fJ [1][2]. SAR ADCs are well-known for power efficiency but their speed is usually limited by the settling of the DAC array and the switching logic. This work describes an interleaved two channels 2b/cycle SAR ADC which adopts a custom-designed capacitor array with high density layout structure to realize a compact DAC implementation, thus reducing the undesired parasitic from routing and density filling. Co-operating with segmentation switching and a low timing skew clock generator, the ADC can achieve GHz sampling rate without any time-interleaved calibration.

ADC Architecture

The ADC architecture and its timing diagram are illustrated in Fig. 1. It consists of a clock generator and two time-interleaved (TI) 2b/cycle SAR ADCs where each channel contains two capacitive binary-weighted DACs (DAC_1 and DAC_2), segmentation switching logic, self-time loop and three comparators. DAC_1 and DAC_2 are utilized as sampling capacitors and simultaneously provide the binary search function for multi-bit quantization. Inputs of the mid-reference comparator are interpolated from DAC_1 and DAC_2 which saves an extra DAC.

During the sampling phase of channel 1 ($\Phi_{s,ch1}$), the differential input signal $\pm V_{in}$ is sampled at the top-plate of $DAC_{1,ch1}$ and $DAC_{2,ch1}$ for high speed operation. Then in the conversion, four clock pulses ($\Phi_{ST,ch1}$) are generated from the self-time loop for 3 comparators and each pulse resolves 2 bit resolution. Channel 2 operates in a similar time interleaving manner. Eventually, both 8 bit codes from channel 1 and 2 are combined within the multiplexer to obtain the final codes.

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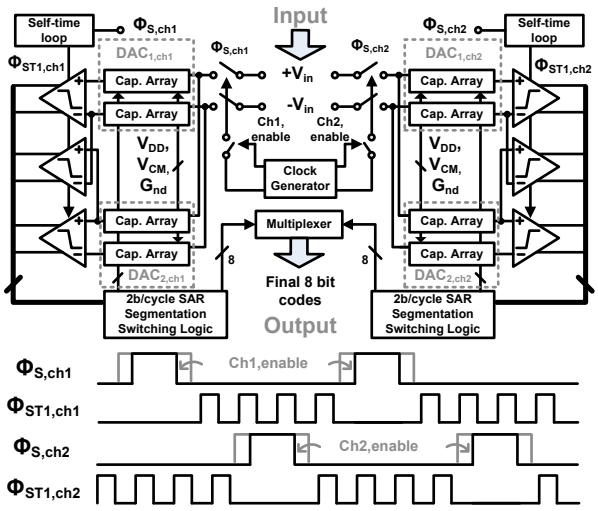

Fig. 1 Overall ADC architecture and its timing diagram.

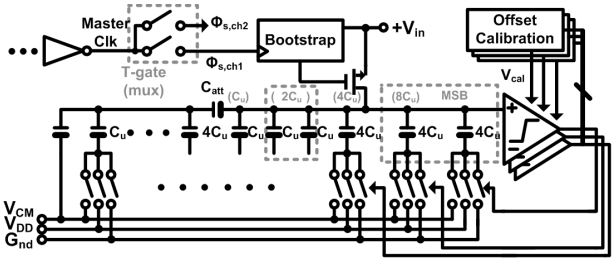

Fig. 2 Detailed single channel (only one cap. array is shown).

Circuit Implementation and Layout

The detailed single channel block diagram is shown in Fig. 2 with one DAC. The sampling front-end utilizes bootstrapped switches to shorten the sampling time and improve the linearity. The timing skew error is minimized by placing the sampling switches of TI channels close to each other and only splitting the master clock just before these switches with a large sizing transmission-gate de-multiplexer. The comparator is a two-stage dynamic topology [3] which has low noise and low power consumption, and offset is calibrated in the foreground with unbalanced triode region loads.

A segmentation switching scheme is utilized in this design. By splitting the even bit capacitors into two identical segments, each comparator's outputs only control the bottom-plate of a capacitor segment in each 2b quantization. Specific allocation is done in the DAC array to achieve optimum arrangement for 2b/cycle comparator's outputs, which reduces the comparators' loading, routing and extra logics of the binary switching. All logic circuits are implemented with dynamic gates for high-speed and low-power operation. Pre-charge and decision logics are also combined, which saves redundant logic and buffer switching power. Plus, a low-Vt transistor is used to further reduce the critical path delay in the SA loop.

The custom-designed unit capacitor structure is depicted in Fig. 3 (a). It consists of multiple layers of crossing metals which maximize the intended capacitance in certain area while lessen the undesired fringing field coupling, and its two-way systematical structure guarantees a good matching nature over the peripheral effect. A 3×3 configuration are shown, while 5× 7 is implemented in this design with 5 layers which are optimized for the density DRC rule. A split capacitor structure is utilized at the DAC for area and power optimization. Fig. 3 (b) indicates a layout example of the split structure where the top-plate of each unit capacitor is shared thus adding no extra routing parasitic capacitance. A common-centroid structure is used to avoid the systematic mismatch error. As a result, no metal filling is needed within the DAC area thus yielding a unit capacitance C_u of 2.6fF by adjusting its dimensions. Comparing with the custom fringe structure under the same area and number of metal layers, a 31% increase in the overall capacitance value is achieved, with 24% less top and 33% less bottom plate parasitic, as it is observed from the extracted result of the design. The routing distance between the attenuation capacitor (C_{att}) and the MSB sub-array is minimized and its square structure allows short routing distance from the bottom-plate of the capacitor to the control switches. This structure yields a very compact DAC layout that greatly minimizes the undesired routing parasitic, thus enhancing speed and saving power. On the other hand, the C_{att} is adjusted to compensate the non-linearity effect caused by the split structure being its amount estimated from the extraction, which can tolerant around 10 % top-plate parasitic variation.

Measurement Results

The prototype is realized in 1P7M 65nm CMOS, occupying a core area of 0.0086mm^2 and an on-chip calibration area of 0.0041mm^2, as shown in Fig. 4, with a partially zoomed-in layout. The ADC operates at 1GS/s, under 1V supply, consuming 3.8mW. The analog power, including S/H, comparators and switching is 1.8mW and the digital power, including the clock generator, SA logic and calibration is 2mW.

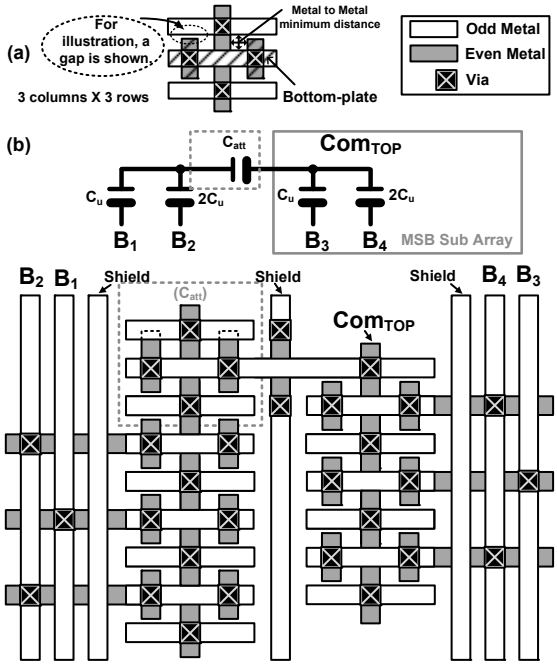

Fig. 3 (a) Unit cap. structure. (b) 4bit split DAC layout example.

Fig. 5 shows the measured SNDR histogram, obtained with a low frequency input, of 20 chips with the same configuration. No splitting and timing skew tones are observed within the chips. By selecting the one with the mean SNDR performance among 20 chips to report the results, the measured spectrum near the Nyquist input is indicated in Fig. 6 and, the SFDR and SNDR versus input frequency is exhibited in Fig. 7. The SNDR at DC is 45.77dB, while it drops to 42.75dB with a 520MHz input frequency. The maximum INL/DNL is -23.7/26.7 LSB and 0.76/-0.85 LSB, before and after on-chip offset calibration, respectively. The performance summary and a benchmark with state-of-the-art ADCs are shown in Table I, with the ADC achieving a FoM (Power/$2^{ENOB@DC} \times f_s$) of 24fJ.

Acknowledgements

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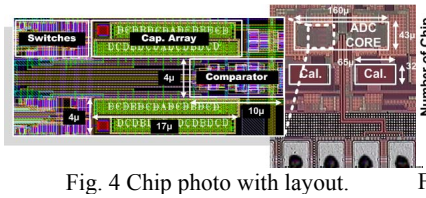

Fig. 4 Chip photo with layout.

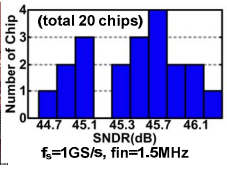

Fig. 5 SNDR histogram.

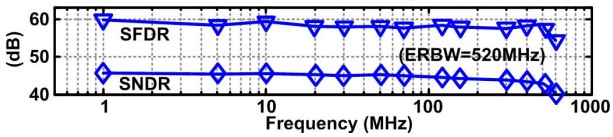

Fig. 6 Measured SNDR and SFDR versus input frequency.

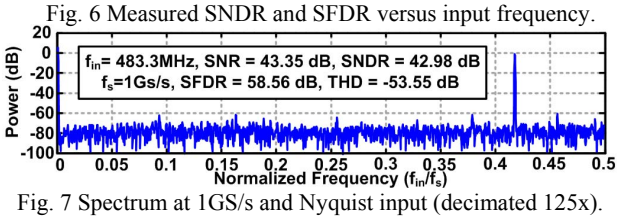

Fig. 7 Spectrum at 1GS/s and Nyquist input (decimated 125x).

TABLE I : Performance Summary and Benchmark

	[4] VLSI' 08	[5] ISSCC'09	[2] VLSI' 11	[1] VLSI' 11	This Work
Architecture	Ti-Pipeline	Ti-SAR	Sub-ranging	Pipeline	Ti-SAR
Technology (nm)	65	45	55	45	65
Resolution(bit)	8	7	8	7	8
Sampling Rate(GS/s)	0.8	2.5	1.0	1.3	1.0
Supply Voltage (V)	1.2	1.1	1.2	1.2	1.0
ENOB@Nquist(dB)	7.05	5.4	6.2	5.2	6.8
DNL/INL(LSB)	0.16/0.23	0.5/0.8	0.8/1.2	<1/1	0.76/0.85
Power (mW)	30	50	16	22	3.8
FoM (fJ/conv-step)	187	480	125	190	24
Area(mm^2)	0.12	1.0	0.2	0.023	0.013