A 0.024 mm^2 4.9 fJ 10-bit 2 MS/s SAR ADC in 65 nm CMOS

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***Abstract*—This paper presents a Successive Approximation Register Analog-to-Digital Converter (SAR ADC) design for sensor applications. An energy-saving switching technique is proposed to achieve ultra low power consumption. The measured Signal-to-Noise-and-Distortion Ratio (SNDR) of the ADC is 58.4 dB at 2 MS/s with an ultra-low power consumption of only 6.6 μW from a 0.8V supply, resulting in a Figure-Of-Merit (FOM) of 4.9 fJ/conversion-step. The prototype is fabricated in 65 nm CMOS technology with an area of 0.024 mm^2.**

Keywords- Analgo-to-Digital converter; ultra-low power; Successive Approximation Register; sensor applications.

I. INTRODUCTION

Highly efficient Analog-to-Digital Converters (ADCs) have been commonly employed for power management and sensor applications such as, battery measurement systems, touch screen, and Micro-Electro-Mechanical Systems (MEMS), operating from a few hundreds of kS/s to several MS/s [1]. To cope with the applications, ADCs with Mega-Hertz conversion rate and ultra-low power are highly demanded. The Successive Approximation Register (SAR) ADC architecture is well suited for those applications due to its moderate speed, medium to high resolution and very low-power consumption.

The conventional N-bit charge redistribution SAR ADC consists of an N-bit binary-weighted capacitive DAC array with voltage switches, a comparator and a SAR control logic, as shown in Fig. 1. This architecture uses the binary search method to determine the configuration of bits during the conversion. The output voltage of the DAC array (V_X) is charged by connecting the bottom plate of the capacitors to either ground or V_{ref}, and then the decoding binary code is determined by comparing the voltage V_X with ground. The conversion starts from the MSB capacitor and repeats towards the LSB one, until all codes are decoded. For a N-bit SAR ADC, the capacitive array consists of N+1 capacitors with the values of $2^{N-1}C_0$ (MSB) and C_0 (LSB), with C_0 as the unit capacitance. The switching energy for decoding the MSB would be as large as 2^{N-1} times that of decoding the LSB. The conventional method charges and discharges the MSB or a larger capacitance repeatedly, and consumes a great amount of power.

The primary source of power consumption in a SAR ADC is from charging/discharging the capacitive array, as well as the digital logic circuit. Recently, several energy-efficient switching methods, such as the split capacitor [2] and the Vcm–based switching [3], have been proposed to minimize the switching energy of the capacitor network. Although these methods reduce the switching energy of the capacitive array, they complicate the SAR logic thus leading to an increased number of capacitors and switches.

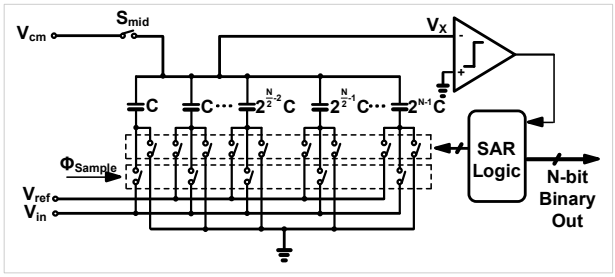

Fig.1. A conventional 10-bit SAR ADC architecture

This paper proposes a new energy-saving switching technique to achieve low power consumption in SAR ADC. By altering slightly the conventional switching network and SAR logic, and determining the MSB codes in the smaller capacitors instead of in the larger ones, this technique can save DAC array switching energy efficiently and draws a little extra digital power consumption.

II. PROPOSED ADC ARCHITECTURE

The architecture of the proposed 10-bit SAR ADC is shown in Fig. 2. It comprises a capacitive DAC array with switches, a dynamic comparator and SAR control logic. The capacitive DAC array is composed by 10-bit split schemes. The comparator determines the value of each bit by comparing the voltages of the DAC array. The SAR logic controls the DAC operations to perform the binary-scaled feedback during the successive approximation cycle, with all control signals derived from the clock generator.

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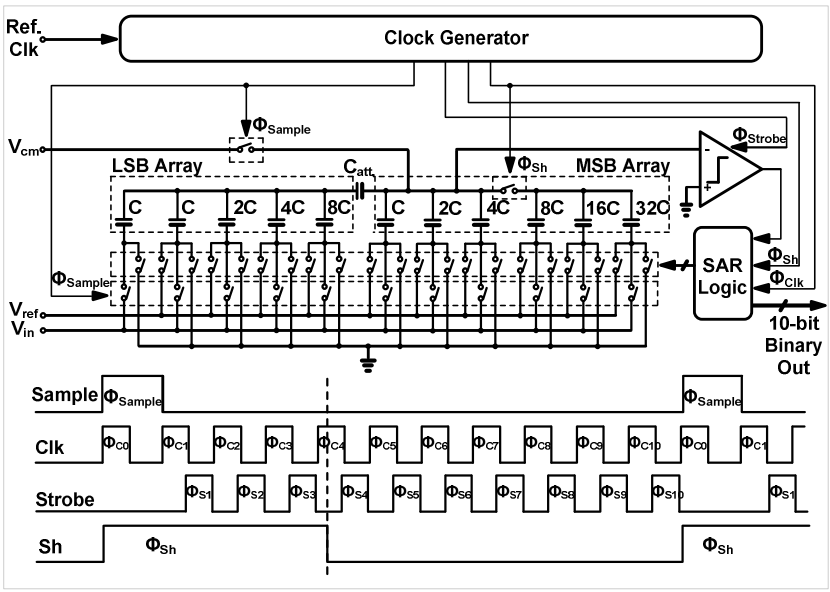

Fig.2. Proposed ADC circuit and timing diagram

In this architecture as shown in Fig. 2, only two analog switches in the top plate of the capacitor array and 38 digital switches in the SAR control logic are added when compared with the conventional one. The capacitive array includes the LSB (C to 4C) and MSB (C to 32C) array. The MSB array is divided in two parts: 3-bit small capacitor (C to 4C) and 3-bit large capacitor (8C to 32C) array, through the switching of a transmission gate. The digital switches implemented with minimum size transistors do not consume too much power, and the proposed method only needs to draw a reduced extra value of digital power.

III. PROPOSED SWITCHING SCHEME

A. Operating Principle

In the conventional SAR ADC, the binary codes are generated by switching from the largest capacitor to the smallest one, on the contrary, the conversion in the proposed architecture does not start from the largest capacitor.

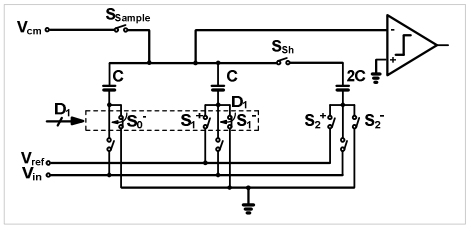

Fig.3. First conversion in the small capacitor (Second step)

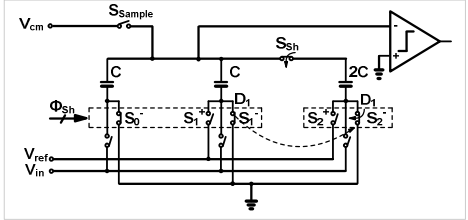

Fig.4. Bit shift (Third step)

Fig. 3 and Fig. 4 show an example of a 2-bit SAR ADC with the proposed switching diagram. In the sampling phase, the switches S_{sh} and S_{Sample} are off and the whole DAC array samples the input signal. In the second step as shown in Fig. 3, the switches S_{sh} and S_{Sample} are on, the first bit converts with the small capacitor 'Cw' instead of the large one "2C" in the conventional method. If the conversion result is '1' from the comparator, the capacitor 'C' keeps the Vref value. In Fig. 3, the conversion result D_1 is '0', the switch S_1^- is turned off and the capacitor 'C' connects to ground.

In the third step, as shown in Fig. 4, the switch S_{sh} is turned off, and the first bit D_1 shifts to the large capacitor '2C' from the small 'C', this means that the switch S_2^- is turned off and the capacitor '2C' will connect to ground directly. This completes the conversion cycle without requiring any additional cycle. In the fourth step, the second bit is obtained with the small capacitor 'C', sequentially. The 2-bit binary codes are determined.

The timing diagram of the 10-bit ADC is shown in Fig. 2. Initially, the capacitive DAC array samples the input signal with the bootstrapped switch in the "Φ_{Sample}" clock phase. After sampling, the "Clk" and the "Strobe" activate the SAR logic and the comparator, respectively, to perform the 3-bit conversion with the small capacitors. Then, the switch Φ_{Sh} is turned off and the 3-bit codes shift from the small capacitors to the large ones. After bit shifting, the DAC array starts subsequently the other 7-bit conversions.

B. Energy Evaluation

This switching technique is simple with two advantages in terms of saving switching energy: first, the first-step conversion is completed in the smaller capacitor instead of the larger; second, if the first bit code is zero, it is not necessary to

charge the large capacitor. Both of these actions can save a significant amount of power.

For the conventional 2-bit SAR ADC, the total switching energy for completing the 4 codes “00” “01” “10” and “11” is [2]:

$$E_{con}^{'} = \frac{5}{2} CV_{ref}{}^{2} + 4\beta CV_{ref}{}^{2} \quad (1)$$

Where C is the unit capacitance, V_{ref} is the reference voltage, and β is the ratio of bottom parasitic of the unit capacitor.

For the proposed technique, the total switching energy is:

$$E_{bsh}^{'} = \frac{3}{2} CV_{ref}{}^{2} + 3\beta CV_{ref}{}^{2} \quad (2)$$

Therefore, if the β is about 0.6 (got this value from extracting the layout parasitic in Cadence), this technique grants a switching energy of 32% in average compared to the conventional switching scheme.

For a 10-bit SAR ADC, this technique grants a switching energy of 15% in average. It cannot achieve more savings in switching power, because shifting the digital codes from 3-bit small capacitor array (C to 4C) to 3-bit large capacitor array (8C to 32C) consumes a large amount of power. With the worst case when the 6-bit digital codes are “111 111”, and to convert them, the switching energy is:

$$E_{bsh1} = \frac{3339}{64} CV_{ref}{}^{2} + 66\beta CV_{ref}{}^{2} \quad (3)$$

In equation (3), the switching energy of shifting the 3-bit digital codes with “111” from the small (C to 4C) to large (8C to 32C) capacitor array consumes too much power. However, for the traditional SAR ADC, the switching energy only is:

$$E_{con1} = \frac{1365}{64} CV_{ref}{}^{2} + 63\beta CV_{ref}{}^{2} \quad (4)$$

The traditional does not shift the 3-bit digital code, and can save power compared with the proposed in worst case.

However, with the best case when the 6-bit digital codes are “000 000”, the switching energy is:

$$E_{bsh0} = \frac{707}{64} CV_{ref}{}^{2} + 14\beta CV_{ref}{}^{2} \quad (5)$$

Shifting the 3-bit digital codes with “000” does not consume any power. But, for the traditional, the switching energy is:

$$E_{con0} = \frac{2667}{64} CV_{ref}{}^{2} + 63\beta CV_{ref}{}^{2} \quad (6)$$

The proposed technique saves power compared with the traditional in the best case. At last, the energy efficiency for this technique is limited to 15% in average.

IV. Circuit Implementation

A. Capacitive Array

Fig. 2 shows the circuit of the proposed 10-bit SAR ADC. To lower the power of the capacitive DAC array, and decrease the number of unit capacitor, the binary capacitors are scaled down with the attenuation capacitor ($C_{att.}$). Due to the top-plate parasitic effect of the LSB array $C_{att.}$ need to be optimized. The MSB and LSB arrays are composed of 63 and 16 unit capacitors, respectively.

The DAC array (64C) samples the input signal in the proposed ADC. If only thermal noise is concerned, the required sampling capacitance is 82 fF (For a SNR 65 dB with supply voltage 0.8 V), and it means that the unit capacitance is not less than 1.3 fF. Also, in order to neutralize the capacitor process variation, the unit capacitor is implemented by fringing capacitor with capacitance of 7.7 fF.

B. Comparator

The comparator resolution becomes a key in ADC design since the voltage value of 1 LSB decreases with the supply voltage. In the proposed ADC, the switching technique does not increase the requirements of the comparator. The comparator circuit, without the pre-amplifier, is employed by the dynamic latch as shown in Fig. 5.

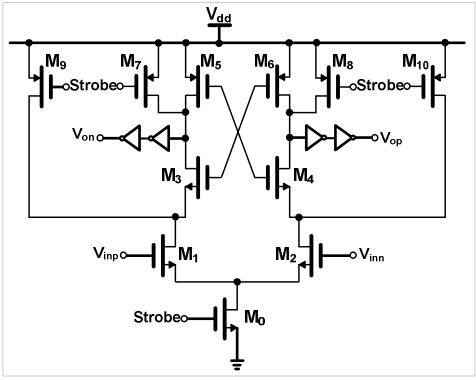

Fig.5. Dynamic comparator

C. Successive Approximation Registers

The SAR logic provides the self-timed controlling clock pulses in each approximation cycle, and it is composed by a shift register, bit register and a switching logic block. The shift register, which consists of low power D-Flip-Flops, generates the bit cycle. The bit register, which contains the dynamic circuit, detects each bit decision from the comparator, thus locks it for the next stage of processing. Besides, the extra-38 digital switches in the SAR logic are used to control the bits shifted from the small to the large capacitors.

In the digital circuit, the clock generator consumes most of the power (around 52% of the total power). Extra 38 minimum size digital switches are added, with the new technique, when compared with the conventional, leading to an additional power consumption of less than 0.1%, therefore, not increasing the circuit complexity and saving power efficiently.

V. Measurement Results

The proposed SAR ADC is fabricated in a 65 nm CMOS process with high threshold option. The full micrograph and the zoomed-in view of the core are shown in Fig. 6. The total area of the chip is 1x1 mm^2 with the ADC core taking up only 220x110 μm^2.

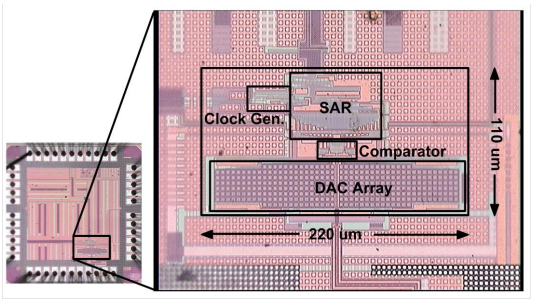

Fig.6. Chip micrograph

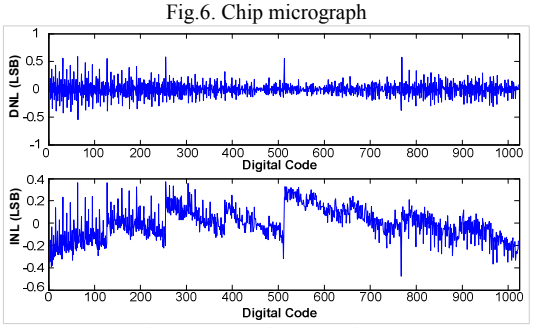

Fig.7. Measured DNL and INL

The static performance is characterized through the differential nonlinearity (DNL) and integral nonlinearity (INL). As shown in Fig. 7, the DNL and INL are +0.59/-0.55 LSB and +0.37/-0.48 LSB @ 2 MS/s, respectively. Fig. 8 shows the frequency spectrum with low and high input frequencies from 0.8 V supply. Fig. 9 plots the measured SNDR versus the input frequency.

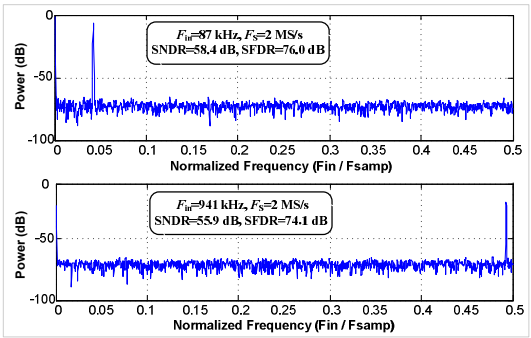

Fig.8. Measured FFT spectrum at low and high input frequencies

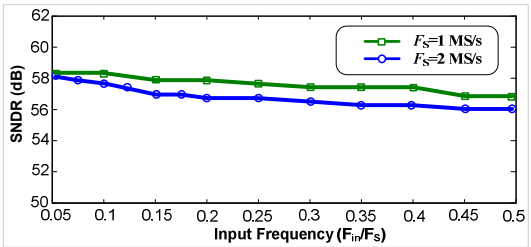

Fig.9. Measured SNDR vs. input frequency.

TABLE I. Performance Summary and Benchmark

Specifications	JSSC'11 [4]	ISSCC'08 [5]	VLSI'10 [6]	This Work	
Technology	0.18μm	65nm	0.18μm	65nm	
Resolution (bits)	10	10	10	10	
Input range	Rail-to-rail	1.25V$_{pp}$	N/A	Rail-to-rail	
Sampling Rate (MS/s)	0.1	1	10	2	
Supply voltage (V)	0.6	1.0	1.0	0.8	0.7/0.6*
SNDR (dB)	57.7	54.4	60.29	58.4	57.7
Power (μW)	1.3	1.9	98	6.6	2.0
FOM (fJ/Conv.-s)	21	4.4	11	4.9	3.9
DNL (LSB)	+0.4/-0.7	0.5	+0.3/-0.3	+0.59/-0.55	
INL (LSB)	+0.8/-0.7	2.2	+0.2/-0.4	+0.37/-0.48	
Active Area (mm^2)	0.125	0.026	0.086	0.024	

*Digital supply voltage 0.7 V and analog one 0.6 V.

The ADC consumes 6.6 μW from both analog and digital 0.8 V supply voltage at a conversion rate of 2 MS/s. The comparator, DAC, and digital SAR consume approximately 13%, 38% and 49% of power, respectively.

The measured results show that the circuit can work with a supply voltage range from 0.6 V to 1 V. The ADC draws only 2.0 μW from digital 0.7 V and analog 0.6 V supply voltage at a conversion rate of 2 MS/s. Considering a Figure-Of-Merit (FOM) defined by FOM = Power/(2^{ENOB}*fs), this work can achieve a peak FOM of 3.9 fJ/conversion-step at 2 MS/s.

The ADC performance and benchmark with the state-of-the-art ADCs are summarized in Table I.

VI. Conclusions

This paper proposes an efficient switching technique which consumes low switching energy with no extra circuit complexity. The prototype ADC fabricated in 65 nm CMOS occupies an active area of only 0.024 mm^2 and operates well under 0.8 V supply voltage. The ADC draws only 2.0 μW power from a digital supply voltage of 0.7 V and an analog one of 0.6 V, and has a peak FOM 3.9 fJ/Conversion-step at 2 MS/s

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