

A 1.8-V 1.056-GS/S 6-B FLASH-INTERPOLATION ADC FOR MB-OFDM UWB APPLICATIONS

Jun-Xia Ma, Sai-Weng Sin, Seng-Pan U¹, R.P.Martins²

Analog and Mixed Signal VLSI Laboratory (http://www.fst.umac.mo/lab/ans_vlsi),
Faculty of Science and Technology, University of Macau, Macao, China
(1 – Chipidea Microelectronics, Macao, China)
(2 - on leave from Instituto Superior Técnico / UTL)

ABSTRACT

A 1.056 GS/s, 6-bit flash analog-to-digital converter (ADC) is designed in 0.18- μm CMOS, which is suitable to be used in an OFDM-UWB transceiver. Resistive interpolation and averaging techniques are employed to reduce the Pre-Amplifiers number and to average the offset between them. Monte Carlo simulation results show that the ADC achieves 5.45b ENOB with a 445-MHz input signal and DNL and INL of 0.16 and 0.39 LSB respectively. The analog part and digital part consumes 65.3mW and 22mW from a 1.8-V supply, respectively.

KEY WORDS

High Speed Analog-to-Digital Converter, Flash ADC, Averaging, Interpolation, MB-OFDM UWB

I. INTRODUCTION

There is growing interest in commercial Ultra-Wide Band (UWB) communication systems since FCC opened up 7,500 MHz of spectrum (from 3.1 GHz to 10.6 GHz) for use by UWB devices. This paper deals with the ADC design for the multiband OFDM system. The ADC resolution is determined by the tolerable quantization noise, the AGC resolution, and the level of WLAN interferences that are only partially attenuated by the baseband channel-select filter. In [1], it has been proved that the use 4-bit Effective-Number-Of-Bit (ENOB) for 110/200 Mbps, and a 5-bit ENOB for 480 Mbps is sufficient for MB-OFDM UWB system. Therefore, a well-designed 6-bit ADC with 5-bit ENOB or more will be enough for all the working modes and will fit the UWB application.

ADC is always a power-hungry component for the whole analog front-end of the UWB transceiver. Since the UWB systems are always used in portable devices, low-power designs are therefore of critical importance to extend the battery life. Where maximum sampling rate and low to moderate resolution is required, flash ADCs are good candidates among various choices [2, 3]. However, the major advantages of flash architecture also present its main problem: the number of components

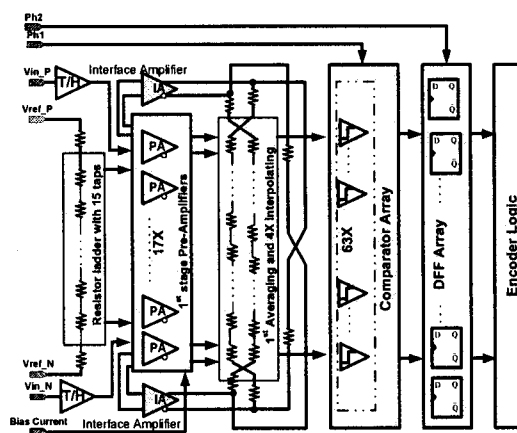


Fig. 1: the 6-b flash-interpolation ADC architecture

increases exponentially with the resolution specifications, leading typically to a large die area and high power consumption. To overcome this problem interpolation technique can be used. Interpolation between reference levels reduces the number of reference taps and preamplifiers resulting in much lower power consumption. The influence of offset voltages in the preamplifiers can be reduced by using averaging between active amplifier stages while at the same time the Signal-to-Noise Ratio (SNR) can be improved without additional power consumption.

With 1.056 GS/s sampling frequency and an ENOB of 5.45 bits at an input signal frequency of 445 MHz, the ADC fulfils the different data rates requirements of the MB-OFDM system. Due to its large ERBW different receiver topologies, like low-IF or zero-IF can be supported. However, the ADC will not be limited to only these applications; for example, it can also be used in the disk-drive read channels.

This paper is organized as follows: section II illustrates the flash ADC architecture and the key ideas to improve the linearity and reduce the power consumption. Section III describes and explains the circuit implementation of the main building blocks. Then in Section IV simulation results are provided to verify the effectiveness of the design and to demonstrate the performance of the ADC. Finally the conclusions are drawn in Section V.

preamplifier stages and does not require the addition of a special resistor component to a pure digital process. By careful architecture and circuit selection, this 4× interpolation, 6-bit, 1.056GS/s flash ADC is realized with only 19 preamplifiers (two for boundary termination) thus resulting in a low power consumption. Interpolation also has a positive effect on the differential non-linearity (DNL) of the ADC [5]. The interpolating resistor string also can be used as the averaging resistor, and in this way a combination of averaging and interpolation is realized in the design.

The offset averaging technique proposed in [6] is an effective method to alleviate the mismatch impact in preamplifier or comparator arrays and, simultaneously, signal-to-noise ratio is improved without additional power consumption. Averaging is achieved by inserting ladder resistors between the outputs of adjacent preamplifiers. Although the averaging technique allows the use of small size transistors throughout the design, it also causes problems at the boundaries of the averaging resistor network. At the edge, the zero-crossings shift inward due to the lack of amplifiers outside the boundary, which causes systematic nonlinearity errors. Besides, the number of random components contributing to the averaging is diminished at the boundary and then counteracts the DNL/INL improvement due to averaging.

The traditional way to solve the termination problem is either to use dummy amplifiers [3] or to resort to extra boundary termination circuits [7]. The dummy method needs many dummy preamplifiers to become more effective. Since only a part of the amplifier array and reference range are usable, this method is not power efficient. Although the extra boundary termination circuit consumes less power and area, it only restores the systematic errors when the averaging window is narrow and the boundary issue is less severe. In this paper, a triple-cross connection method [4] is chosen to solve the boundary problem with only two interface amplifiers used, as what is shown in Fig. 1. The two crossings at the boundaries minimize the zero-crossing shifts and the third crossing is for proper termination of the resistor network.

C. High Speed Comparator

The circuit for the high speed low power comparator [8] is shown in Fig. 4. This comparator has two operating states, evaluation phase and reset phase. During evaluation phase, V_{latch} is logically high and the current source M_0 turns on, the input devices $M_{1,2}$ sense the differential input, the imbalance potential on V_{out}^+ and V_{out}^- is then regenerated to full swing. In reset phase, M_0 turns off and all reset transistors M_7-M_{12} turn on. The reset devices M_7-M_{12} eliminate all imbalance charge, so the previous data is cleared. The input referred offset of the comparator due to device mismatch can be made relatively small by the preceding gain stage and the averaging technique; therefore we can use small size transistors to ensure high-speed operation.

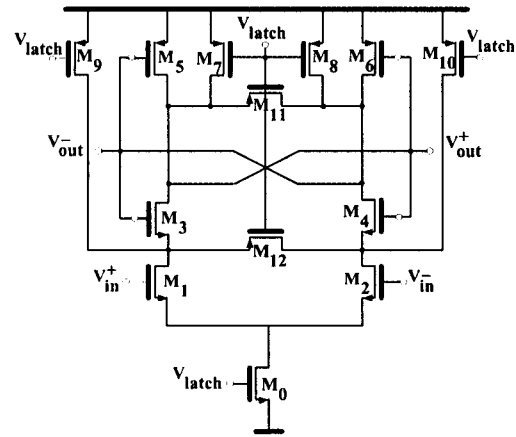


Fig. 4: High speed dynamic comparator

IV. SIMULATION RESULTS

The flash-interpolation ADC has been implemented using a 0.18- μm CMOS process and simulated at circuit-level. The effectiveness of the ADC with averaging and interpolating techniques has been verified comprehensively by Spectre simulator with the components' mismatch effect considered. Fig. 5 shows the simulated DNL and INL from one case of Monte-Carlo simulations, with typical DNL/INL value of 0.39/0.16 LSB, respectively. In addition to static parameters, the dynamic performance of the flash ADC is obtained through an extensive Monte-Carlo simulation using an input signal of 445 MHz and sampling frequency of 1.056 GS/s, with the spectrum for one case presented in Fig. 6. Fig. 7 illustrates the corresponding histogram where the ADC achieves a mean SNDR of 34.578 dB (corresponding to an ENOB of 5.45 bits).

In Fig. 8, the same Monte Carlo simulation is done for 1.056GS/s at the same bias current for different input frequency. SNDR starts at 35.79dB for low frequencies,

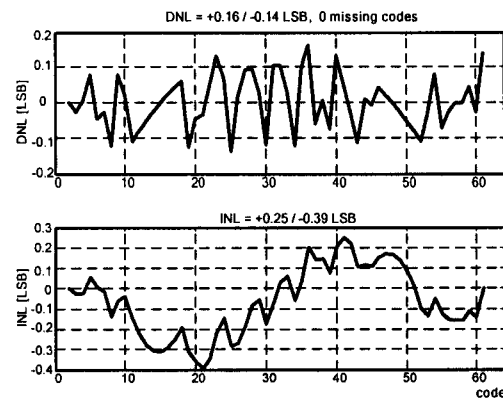


Fig. 5: Simulated DNL and INL of the flash ADC

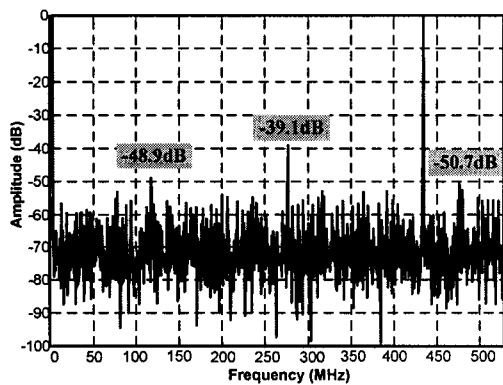


Fig. 6: FFT of a 445 MHz input signal @ 1.056 GS/s

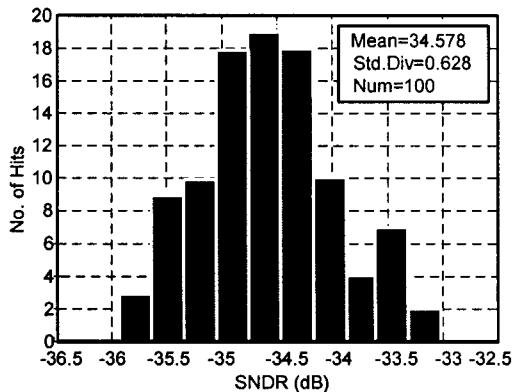


Fig. 7: Histogram of SNDR @ $f_{in}=445.5$ MHz

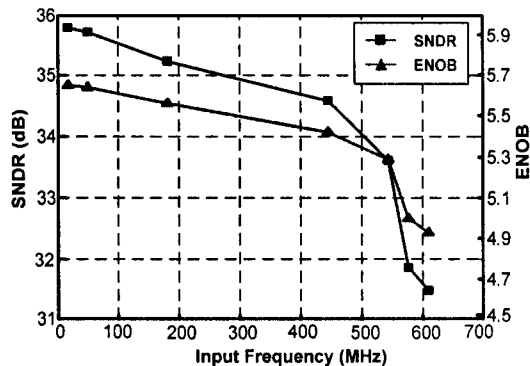


Fig. 8: ENOB versus input frequency

dropping by 3dB at an ERBW of 550MHz. The performance of the whole ADC is summarized in Table I. The power consumption of the converter is 87.3mW in total.

V. CONCLUSIONS

In this paper the architecture, circuit and simulation results of a 1.056 GS/s 6-b flash-interpolation ADC have been presented. A triple-cross connection method has been adopted to improve the offset averaging efficiency. Open-loop T/Hs are included to ensure the dynamic performance up to Nyquist frequencies. This ADC is optimized to achieve a state-of-the-art figure-of-

merit, defined as $(\text{Power}) / (2^{\text{ENOB}} \cdot 2 \cdot \text{ERBW})$, of 1.2pJ per conversion step. The simulation results show that the ADC fulfills the requirements of the MB-OFDM UWB receiver.

TABLE I : PERFORMANCE SUMMARY OF THE ADC

Parameter		Performance
Supply voltage		1.8 V
Input range (diff.)		1.6V _{P.P} (±800mV)
Sampling Frequency		1.056 GS/s
DNL/INL		0.16LSB/ 0.39 LSB
ENOB	@ $f_{in}=49.5$ MHz	5.64 b
	@ $f_{in}=445$ MHz	5.45 b
Power Consumption	Track and Hold	15.3 mW
	Analog Part (without T/H)	50m W
	Digital Part	22mW

ACKNOWLEDGMENT

This work was financially supported by the *University of Macau* under the research grant with Ref no: RG 027/04-05S/MR/FST.

REFERENCES

- [1] J. Balakrishnan, A. Batra and A. Dabak, "A multi-band OFDM system for UWB Communication," *Ultra Wideband Systems and Technologies, 2003 IEEE Conference*, pp. 354 – 358, Nov. 2003.
- [2] Koen Uyttenhove and Michiel S. J. Steyaert, "A 1.8-V 6-Bit 1.3-GHz Flash ADC in 0.25- μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no.7, pp.1115 – 1122, July 2003
- [3] Michael Choi and Asad A. Abidi, "A 6-b 1.3-Gsample/s A/D converter in 0.35- μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 36, no.12, pp. 1847 – 1858, Dec. 2001.
- [4] Xicheng Jiang, Chang, M.-C.F., "A 1-GHz signal bandwidth 6-bit CMOS ADC with power-efficient averaging," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 532 – 535, Feb. 2005.
- [5] Rudy van de Plassche, *CMOS integrated analog-to-digital and digital-to-analog converters*, Kluwer Academic Publishers, 2003.
- [6] K. Kattmann and J.Barrow, "A technique for reducing differential nonlinearity errors in flash ADCs," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech.*, pp. 170-171, Feb. 1991.
- [7] Scholtens, P.C.S.; Vertregt, M., "A 6-b 1.6-Gsample/s flash ADC in 0.18- μ m CMOS using averaging termination," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1599 - 1609, Dec. 2002.
- [8] J. Montanaro, *et al.*, "A 160-MHz, 32-b, 0.5-W CMOS RISC microprocessor," *IEEE J. Solid-State Circuits*, vol. 31, no. 11. pp.1703-1714, Nov. 1996.
- [9] D. Wei, D. Sun, and A.Abidi, "A 300-MHz mixed-signal FDTS/DFE disk read channel in 0.6- μ m CMOS," in *IEEE Int. Solid-State Circuits Conf.*, pp. 186 – 187, Feb. 2001.
- [10] P.Pai, A Brewster, and A.Abidi, "A 160-MHz analog front-end IC for EPR-IV PRML magnetic storage read channels," *IEEE J. Solid-State Circuits*, vol. 31, pp.1803-1816, Nov. 1996.
- [11] Yao-Jen Chuang, Hsin-Hung Ou, and Bin-Da Liu, "A novel bubble tolerant thermometer-to-binary encoder for flash A/D converter." *VLSI Design, Automation and Test*, Page(s):315 – 318, 27-29 April 2005.