A 1-V 2.56-MHz Clock-Rate CMOS Multi-bit ΔΣ Modulator with Reset-Opamp Technique and Pseudo Data-Weighted-Averaging for Portable Audio Data Acquisition System

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***Abstract*—In this paper, a 1-V second-order multi-bit (3-bit) ΔΣ modulator with reset-opamp technique is presented. The modulators utilized seven 3-bit current-mode comparators to overcome the turn-on problem of the input switches. Pseudo data-weighted averaging (DWA) technique is also utilized to improve the linearity of the internal digital-to-analog converter (DAC). Improvements are made on the implementations of log-shifter to accommodate low voltage issues. Simulation results show that the modulator achieved 75.55 dB SNDR at 20 kHz signal bandwidth and 2.56-MHz clock rate while consuming 22.6 mW.**

***Keywords*—ΔΣ modulator (SDM), reset-opamp (RO) technique, current-mode quantizer, dynamic element matching (DEM), data-weighted averaging (DWA).**

I. INTRODUCTION

Presently, System On Chip (SoC) design is one of the key issues to achieve low-cost, reduce system size and low power consumption in portable devices. Low supply voltages imply low power consumption in digital signal processing systems and thus become increasingly important [1]. Also, due to the modern technology down-scaling, low supply voltage requirements are also driven by the reliability issue of thin oxide [1]. According to the technology trends for the future in [2], the tendency of the acceptable supply voltage for the future thin oxide is plotted in Fig. 1. Other benefits of supply voltage reduction are the increase of battery working life and the reduction of its size and weight, suitable for portable electronic devices. ΔΣ modulators are good candidates for such low power applications due to its simplicity and insensitivity to components non-idealities. For high-speed systems, multi-bit ΔΣ modulators are frequently used due to its reduced requirements on the over-sampling ratio (OSR) [3].

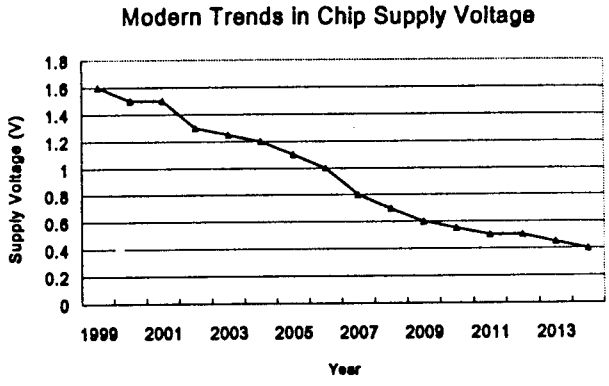

Fig. 1. Estimation trends in supply voltage.

While digital circuits gain great benefits from reduced supply voltages, SoC issues forced analog circuits to be integrated on the same die as the digital parts. Unfortunately, there are great challenges on the low-voltage analog and mixed-signal designs. The analog section of devices is mainly constructed based in switched-capacitor (SC) circuits. Since floating switches cannot operate in low voltage [4], the conventional switched-capacitor circuits suffer from this disadvantage. To overcome this difficulty, several techniques are available, such as switched-opamp [3] and reset-opamp [4] techniques. In this paper, the reset-opamp technique is utilized to implement a 1-V multi-bit sigma-delta (ΔΣ) modulator and in order to achieve faster operation.

Typically, any multi-bit ΔΣ modulator suffers from element mismatch, which can be improved by the Dynamic Element Matching (DEM) algorithm. The traditional data-weighted averaging (DWA), one of DEM techniques, circuits in the 1-V multi-bit ΔΣ modulator suffer from the output level problem. Two new approaches, by using current-mode comparators and the static logics in log-shifter, will be presented to address this issue. Simulation results will be presented to verify the design under such low-voltage (1-V)

environment.

In Section II, the reset-opamp low-voltage techniques are presented. Section III will discuss the design of 1-V multi-bit ΔΣ modulator. And section IV and V will describe the Pseudo DWA and the implementation of the modulator respectively. The simulation performance of the modulator will be shown in section VI. Finally, Section VII makes the conclusion of this paper work.

II. RESET-OPAMP TECHNIQUES

Typical SC circuits suffer from limitations in low voltage (LV) supply. The most serious problem for LV supply is that switches cannot operate properly [4]. This problem can be solved by improving the circuit architectures [4]. Most of them are not truly LV circuit due to internal on-chip high voltage, which can cause the oxide-breakdown problem in modern deep-submicron technology and suffer from speed limitations of the turn-on recovery time for the opamp. Thus, this paper presents an alternative, called reset-opamp technique [4] as shown in Fig. 2. During sampling phase Φ1, the previous opamp is connected as the integrator to transfer the stored charge to the next stage while the next opamp is connected in a unity configuration for the reset and C1 samples the previous stage charge. On the integrated phase Φ2, the previous opamp is reset while the next opamp is connected as an integrator and the sampled charge on C1 is pushed on C2. Since the opamp never switched-off, this can ease the speed requirement of opamps and does not require any recovery time [4].

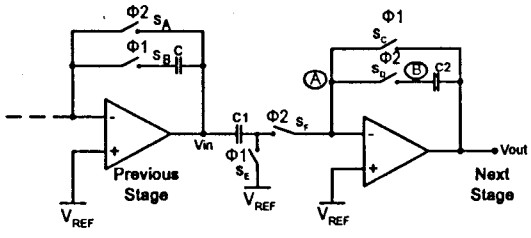

Fig. 2. SC integrator by using reset-opamp technique.

III. 1-V MULTI-BIT ΔΣ MODULATOR ARCHITECTURE

The linearity of a multi-bit ΔΣ modulator is restricted by its internal multi-bit DAC. The errors from the nonidealities in the feedback DAC immersed directly into the input signal and cannot be shaped by the ΔΣ loop. Thus, the precise matching of the DAC unit elements provides a high DAC linearity [5]. Rather than using special physical process to correct the DAC element matching, two other signal-processing strategies can also enhance the linearity: 1) dynamic element matching (DEM) [6], [7] and 2) calibration/ correction using analog [8], [9], digital [10], or mixed-mode [11] schemes. In this paper, DEM is chosen in the multi-bit ΔΣ modulator.

The implementation of any DEM algorithm should be concerned about the clock speed due to the DEM block (element-selection) performs an extra delay in the ΔΣ feedback loop. In an SC implementation, a 3-bit quantizer is typically realized using a 7-level flash ADC and two nonoverlapping clock phases are used [5]. Only a half clock period is available for the generation of the thermometer output code by the DEM building block. Therefore, the delay of DEM must be minimized.

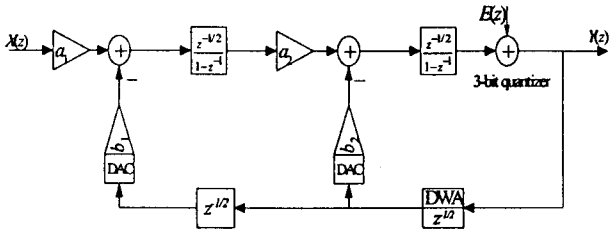

Fig. 3. System building blocks of 3-bit 2nd-order low-pass ΔΣ modulator.

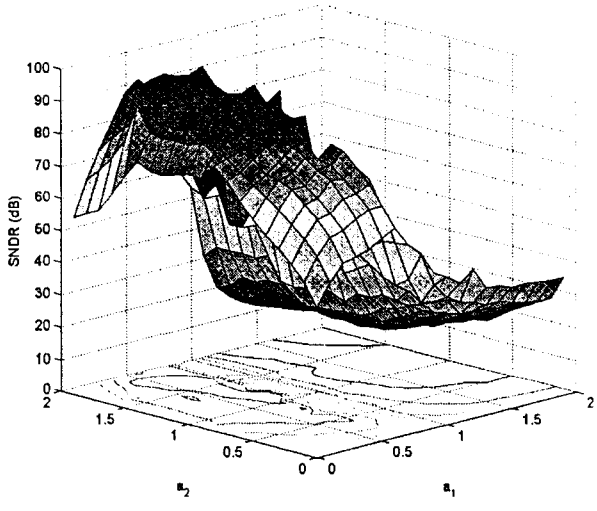

Fig. 4. Determination of the optimal coefficients for 3-bit 2nd-order low-pass ΔΣ modulator.

Data-weighted averaging (DWA) is widely used as the most practical DEM technique to improve the linearity of the internal digital-to-analog converter (DAC), especially for the large number of DAC elements. However, DWA at a low OSR will perform in-band signal-dependent tones that degrade the spurious-free dynamic range. Thus, the DWA algorithm must be modified to prevent these tones. Although the tone problem of DWA can be evaded by the modified versions [12]-[18], these techniques suffer from the

reduction of the signal-to-noise-pulse- distortion ratio (SNDR). This paper presents a simple technique, known as Pseudo DWA, to solve this problem without trade-off with the signal-to-noise ratio (SNR) [5].

The ΔΣ modulator is designed with 3-bit and second-order low-pass performances. A half-delay feedback branch is required to complete ΔΣ function. The overall circuit building blocks are shown in Fig. 3. Before the DAC feedback branches, there are the half-delay and data-weighted averaging (DWA) blocks. For the modeling simulation, the feedback and gain coefficients are optimized as shown in Fig. 4.

IV. Pseudo DWA

A. Pseudo DWA Algorithm

Assume an M-element DAC with input code $y(n)$. In traditional DWA, the DAC unit elements selected at time n are those from $ptr(n)$ to $[ptr(n) + y(n) - 1]$ mod M. The digital register stores the index pointer that the address of the next available unused element. The index pointer is extended modulus M by the DAC input code $y(n)$ [3]

$$ptr(n + 1) = [ptr(n) + y(n)] \bmod M, \qquad (1)$$

The technique presented in this paper, called Pseudo DWA, which is a modified DWA scheme. The LSB of the DAC input code $y(n)$ used to refresh the index pointer in (1) is inverted periodically [5]. The number of clock cycles between such LSB inversion is assumed to be n_{inv}. The element-selection process of Pseudo DWA is similar to the traditional one. The exception is that every n_{inv} clock cycles, a DAC element is either reselected or skipped related to whether the previous DAC input coded was even or odd. By the equation (1), if the corresponding $y(n)$ is even, its LSB inversion will increase $ptr(n + 1)$ by 1. Thus, the Pseudo DWA algorithm will choose DAC elements starting with the next element. Otherwise, if it is odd, $ptr(n + 1)$ will be decreased by 1. Hence, this DWA will choose the previous element. This simple modification to DWA disturbs the periodic nature of the element-selection process and, hence, improves the tone behavior.

B. Comparison of Pseudo DWA to Other DWA Schemes

A number of techniques are available to solve the tone problem in DWA. Fig. 5 and 6 show the performances of three DWA schemes along with the mismatch error and signal level respectively. It shows that DWA algorithms solve the mismatch problem effectively. Although the mismatch error is as large as 5%, they can still perform the correction without degrading SNDR so much. On the other hand, figures also show that Pseudo DWA can achieve a better performance than the traditional DWA and Bi-Directional DWA (Bi-DWA). As a result, Pseudo DWA is used to implement the 3-bit ΔΣ modulator.

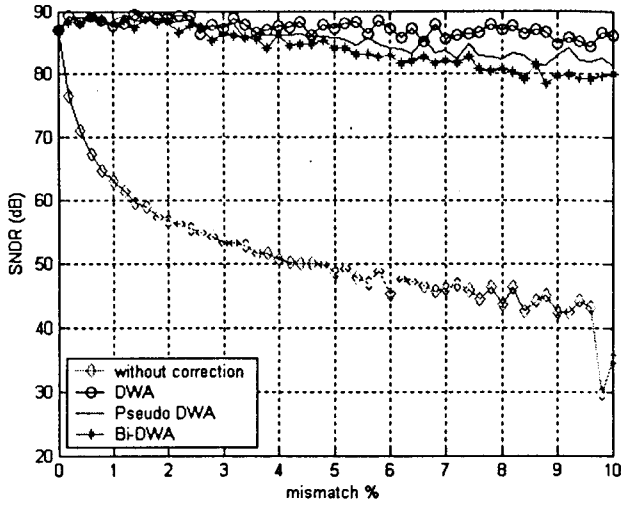

Fig. 5. Effect of mismatch correction on SNDR.

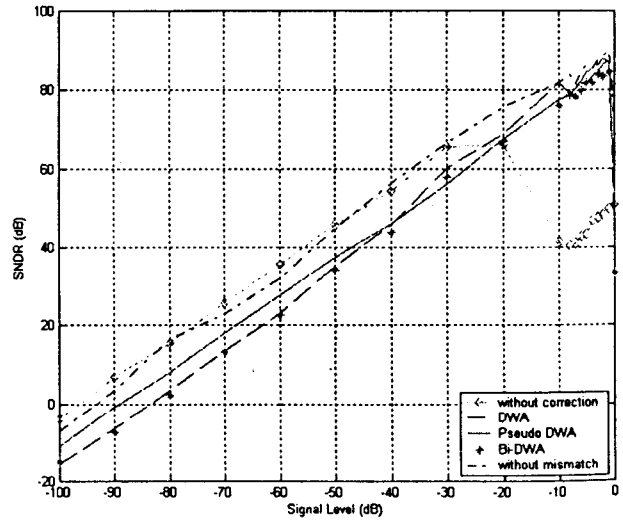

Fig. 6. SNDR vs. signal level under 5% mismatch.

IV. Circuit Level Implementation

The circuit building blocks of the Pseudo DWA algorithm in a ΔΣ ADC with 3-bit quantizer and a 7-element DAC [5] is shown in Fig. 7. A three-stage logarithmic shifter in the ΔΣ feedback path performs the rotation of 7-digit code as the requirement of the Pseudo DWA algorithm. The 3-bit control signal of the shifter depends on the index pointer $ptr_{1\text{-}3}$ and should be stable

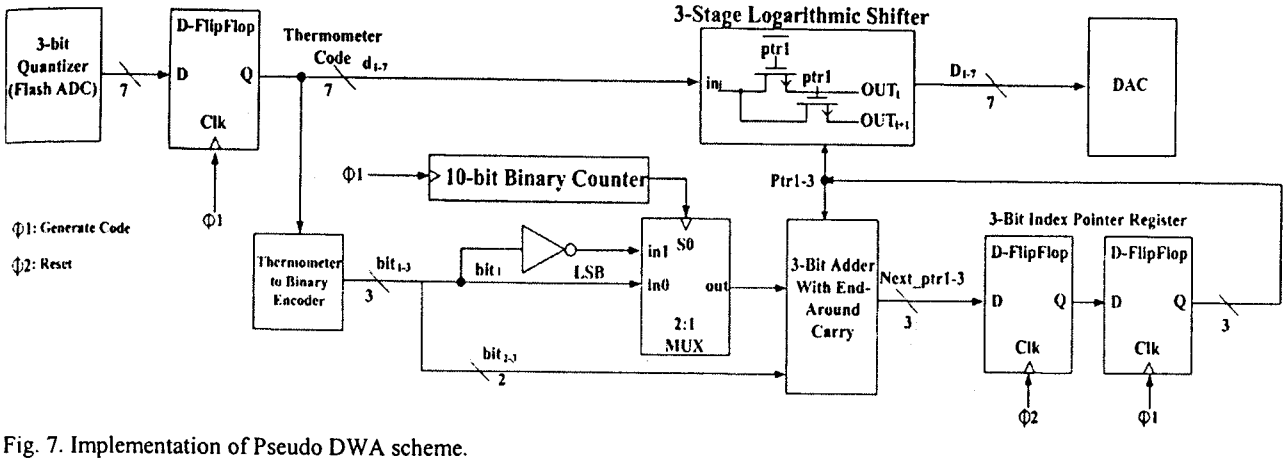

Fig. 7. Implementation of Pseudo DWA scheme.

during phase Φ1 as the thermometer code ripples through the shifter. The index pointer is updated every clock cycle as follows: 1) the 7-digit thermometer output-code d_{1-7} is converted to a 3-bit binary output-code bit_{1-3}; 2) a 3-bit end-around adder increments the index pointer ptr_{1-3} modulus 7 by the output-code bit_{1-3} and generates the next index point $next\_ptr_{1-3}$ (the index pointer to be used at the next Φ1); 3) every 1024 clock cycles, the LSB of the quantizer output-code (bit_1) is inverted before updating the index-pointer register [5]. A 10-bit binary counter and a 2:1 mux control the timing of the LSB inversion. This is the only additional hardware in Pseudo DWA instead of DWA.

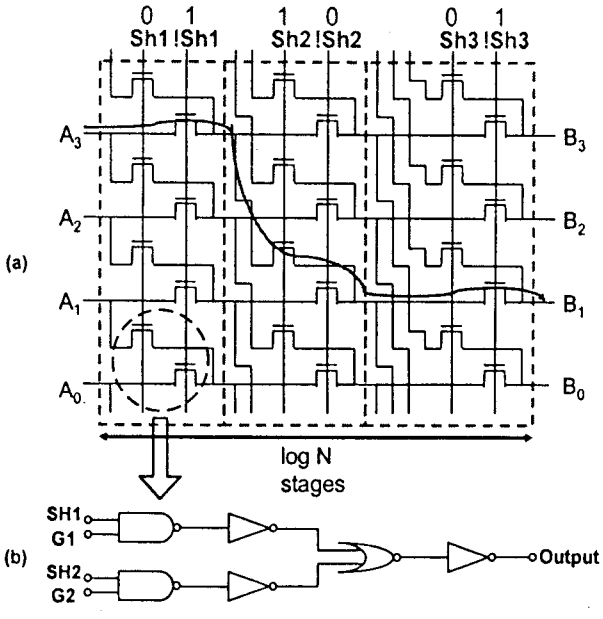

Fig. 8. Gate replacement for the shifter.

The traditional log-shifter, as shown in Fig. 8a, utilized nMOS transistors suffers from that the output of it cannot reach the extreme levels of the supply. This will degrade the performance of the DWA. The proposed log-shifter is based on the static logic gates, which prove proper operation under low supply voltage. Fig. 8b shows the gate implementation of the shifter.

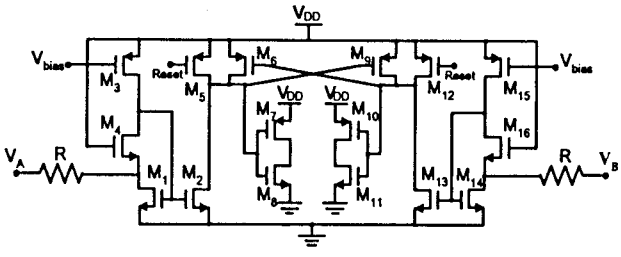

Fig. 9. Half circuit of a current-mode comparator.

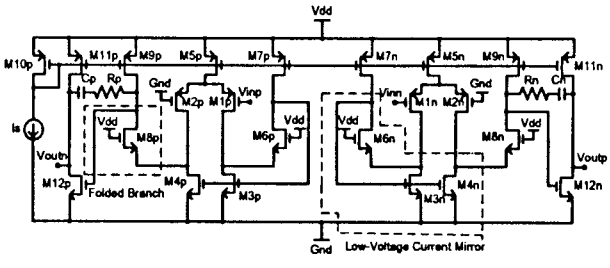

Fig. 10. Low-voltage pseudodifferential operational amplifier.

Since the voltage-mode device has input range problem in low-voltage design, the current-mode comparator can solve this problem. Fig. 9 shows the half circuit of a current-mode comparator. Other benefits of the use of current-mode comparator are that the quantizer can achieve a wider input range. Due to this reason, it does not require any level shifter to adjust the signal level. Therefore, this can ease the circuit complexity and reduce the die size.

In LV voltage supply, it is also hard to implement the internal CMFB circuit to enable the use of fully differential opamps. Fig. 10 shows the structure of a LV pseudodifferential opamp, which enables the efficient implementation of only external CMFB circuit [4].

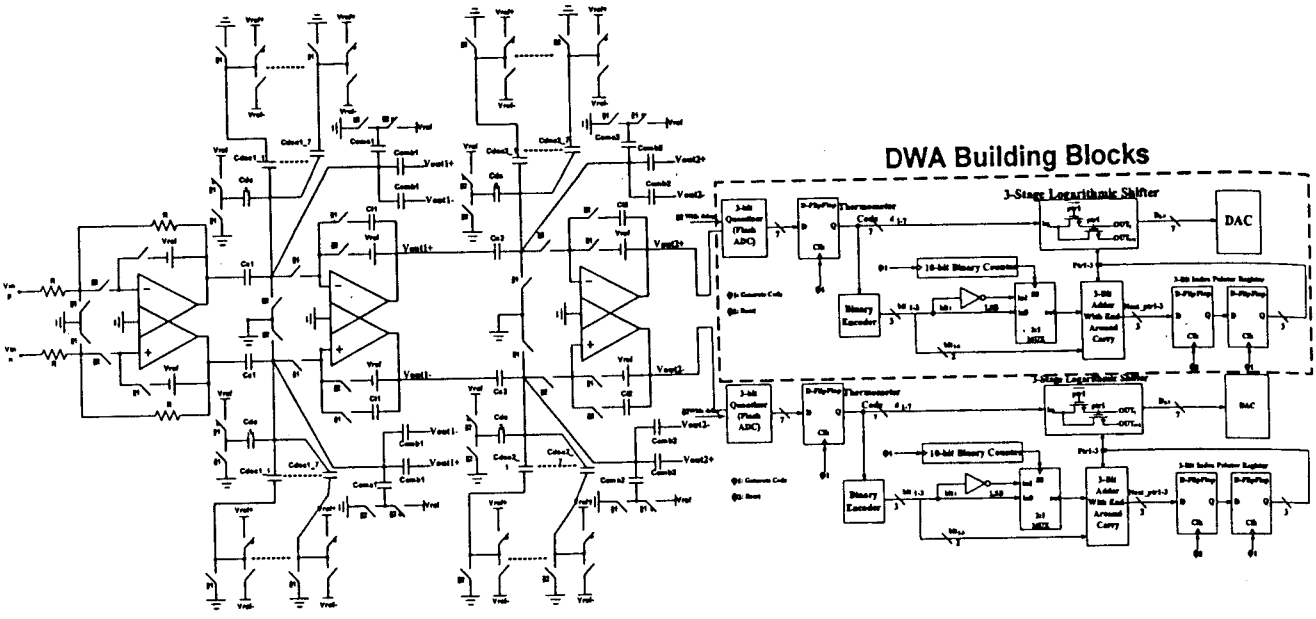

Fig. 11. Overall circuit of 3-bit ΔΣ modulator.

In this LV opamp, two LV techniques are utilized, one is the LV current-mirror in the input stage, and another one is the folded branch which is used to make sure the output stage transistors always operate in their linear region. The key performance results of the LV opamp with a maximum capacitive load of 12 pF are summarized in Table 1. The overall circuit of 3-bit ΔΣ modulator is shown in Fig. 11.

V. Simulation Results

Table. 1. Simulation results of 3-bit ΔΣ modulator.

Supply Voltage	1 V
Signal Bandwidth	20 kHz
Sampling Frequency	2.56 MHz
Max. Diff. Input	1.12 V_{pp}
ENOB	12.3 bits
Peak SNDR	75.55 dB
Power Consumption	22.6 mW

The 3-bit ΔΣ modulator was simulated with a 2.56-MHz clock signal and 1-V supply voltage. Table. 1 summarizes the simulation results. An equivalent number of bits (ENOB) = 12.3 bits was achieved for audio-band (0-20 kHz) operation. Fig. 12a shows its eight-level seven-range digital output. The simulated spectrum of the digital output stream is illustrated in Fig. 12b. No harmonics were simulated.

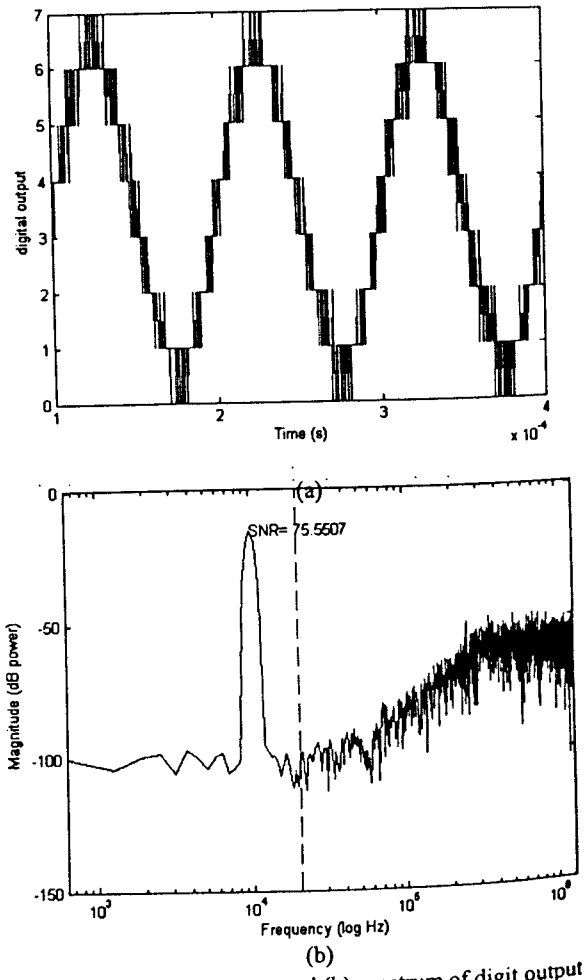

Fig. 12. (a) Transient response and (b) spectrum of digit output of 3-bit ΔΣ modulator.

Table. 2. Low-voltage opamp results.

Adc	fu	PM	$T_{Settling}$	Slew Rate
68 dB	120 MHz	58°	16.5 ns	60 V/μs

VI. CONCLUSION

In this paper, a 1-V multi-bit ΔΣ modulator is implemented using Pseudo DWA algorithm to prevent the occurrence of in-band signal-dependent tones, without sacrificing the signal-to-noise ratio. This implementation adds no extra delay in the ΔΣ feedback loop.

To address the low-voltage issue, reset-opamp technique and current-mode comparator are utilized, and static logic gates are applied in log-shifter to overcome the output range problem.

The low-voltage multi-bit ΔΣ modulator can operate at 1-V and 2.56-MHz clock rate for 20 kHz audio-band. The modulator has a peak SNDR of 75.55 dB for 1.12-V_{pp} and ENOB of 12.3 bits while consuming 22.6 mW.

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