A Multistandard Transmitter D/A Interface with Embedded Frequency Up-Conversion and Two-Step Channel Selection

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Abstract- This paper presents a novel CMOS D/A interface for multi-standard wireless transmitter, embedding a programmable analog-double quadrature sampling (A-DQS) technique for frequency up-conversion and IF channel selection. The I/Q-channel D/A conversion core utilizes a current steering technique to achieve 10-bit resolution and 120-MSample/s satisfying IEEE 802.11a WLANs type-approval. The design and implementation were completed in *Cadence*™ environment based on 0.35-μm CMOS. With 2.5-V analog and 1.8-V digital supplies, the whole die consumes 43 mW. The |INL| and |DNL| are less than 0.42 LSB and 0.38 LSB, respectively. The SFDR is 56dB @ 1MHz and the active chip area is 2.55 mm^2.

Keywords-Analog front-end, analog-double quadrature sampling, quadrature IF transmitter

1. INTRODUCTION

The trend of wireless communications will unite the wireless personal area networks (WPANs), local area networks (WLANs) and wide area networks (WWANs). On the other hand, multistandard wireless transceiver integrated circuits (ICs) will be in an increased demand for future support of all wireless environments with low-power and low-cost CMOS implementations. Unfortunately, the traditional commercial transceiver infrastructures still require some power-hungry off-chip components [1-2] in the overall transceiver architecture. Therefore, they are no longer feasible in required multi-standard communication systems, then contradicting the state-of-the-art scope of System-On-a-Chip (SoC).

This paper uses a two-step channel selection technique, which was originally employed in low-IF/zero-IF wireless receiver [3] for relaxing the frequency synthesizer magnitude matching and phase-noise requirements, and that can be migrated to its transmitter counterpart in order to share identical benefits. Such proposed architecture, as shown in Fig. 1, not only reduces the PLL frequency synthesizer (PLL-FS) magnitude mismatch and phase noise, but also simplifies the analog local oscillator and the digital controller. This paper will be focused in the design and implementation of the transmitter analog front-end (AFE). The targeted application will cover Bluetooth, WCDMA and IEEE 802.11a.

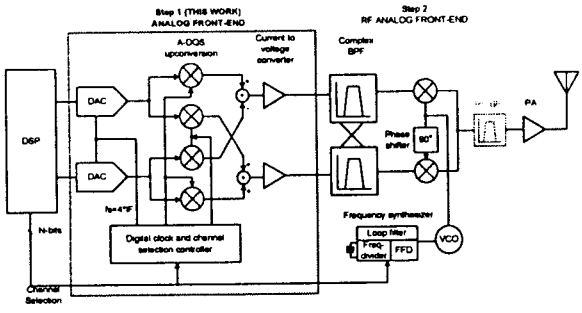

Fig. 1 Proposed two-step channel selection wireless transmitter.

First, the proposed transmitter architecture will be presented in section 2. In section 3, the circuit implementation will be discussed, and the simulation result of the D/A interface will be provided in section 4. Finally, the conclusion will be drawn in section 5.

2. TRANSMITTER ARCHITECTURE

The proposed transmitter architecture is designed based on the quadrature IF up-converter. The baseband-to-intermediate frequency (IF) up-converter has been moved between the current steering DAC and current to voltage converter. It is implemented by the mean of A-DQS technique as Fig. 2. Applying A-DQS up-converter technique, the equivalent digital modulation signal can be generating in continue time. The main benefit is the modulation signal is control easily, high-integrate and power consumption efficiency. The complex up-converted signal will pass through the complex band past filter (BPF), which can smooth the DAC output signal and compress the image signal. As this image is 120MHz away form the signal band, it should be relatively easy to remove. Then, the complex IF signal can be up-converted to real radio frequency (RF) by quadrature mixers. Moreover, the high frequency-band pass filter (HF-BPF) is unnecessary that depend on the quality required.

2.1 A-DQS in transmitter analog front end

Four mixers operate for complex-to-complex frequency conversion namely analog double

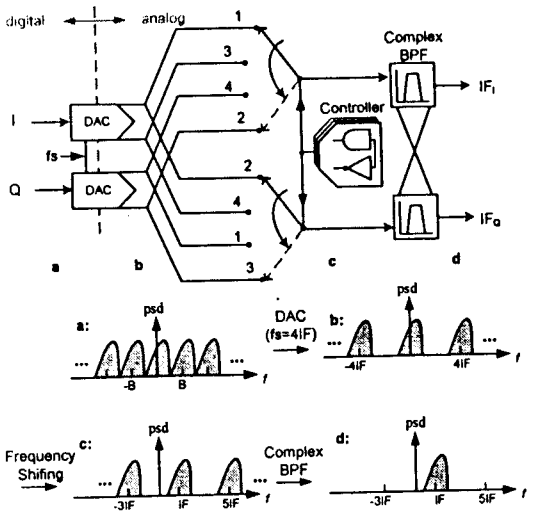

Fig. 2 Proposed A-DQS technique in quadrature IF up-conversion.

quadrature sampling, which has been implemented in the charged mode switch capacitor (SC) down-converter [3]. In this paper, it will be implemented in current mode with up-conversion. The advantage is placing the sampling frequency (f_s) equals to four times the center frequency, the mixers can simplify to digital mixing operation since it then corresponds to digital multiplication by ±1 or 0. Therefore, the up-converter is efficiently embedded into the DAC as using several switches and programmable control circuit. Using digital controller is significant solve the image problem.

2.2 A-DQS channel selection in transmitter

The A-DQS technique is not only simplified the transmitter up-conversion structure, the other attracted function is explored from the shifting characteristic to perform channel selection [4]. The idea is utilizing the forward shifting (FS) or backward shifting (BS) property, so that the complex signal can be shifted to one side of center frequency adjacency by adjusting the switching sequence of digital controller.

The channel selection processing is separated into two steps. The first step is baseband-to-IF up-conversion, it is obviously that one center frequency can carried the baseband signal into two different IF channels by using shifting property. In the second step complex-to-real up-conversion, the phase-lock loop frequency synthesizer transports the intermediate frequency signal to the radio frequency. As a result, the resolution of carrier frequency can be relaxed 50% by applying channel selection idea in the intermediate frequency.

2.3 Design D/A interface

The D/A interface is designed for different standard, they have range 1MHz to 20MHz channel spacing. The digital modulated signal, which is modulated in the back-end, is up-converted to IF by utilizing the A-DQS technique. Two different center frequencies are generated as 0.5× and 1.5× maximum signal bandwidth, i.e., 10MHz and 30MHz respectively. Therefore, the upper limit of D/A interface output frequency is 40MHz.

The 10-bit DAC is utilized to achieve around -60dBc adjacent channel power (ACP). The required sampling rate of A-DQS technique is 4× up-conversion center frequency, thereby, the 120MSample/s oversampling DAC (OSDAR) is designed. This OSDAC can also reduce the constraint of following complex bandpass filter. In the designed transmitter, the complex filter is designed with single-ended input impedance 5kΩ and common mode voltage is 1V.

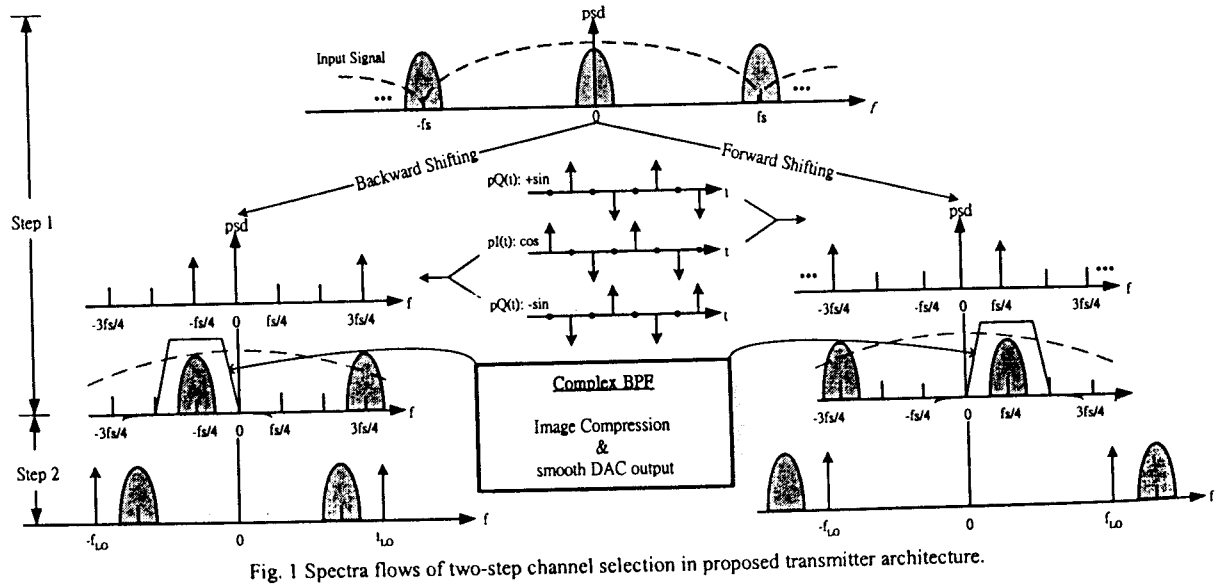

Fig. 1 Spectra flows of two-step channel selection in proposed transmitter architecture.

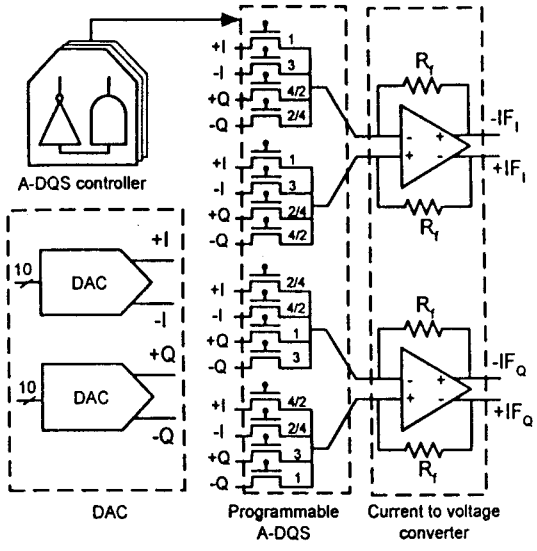

Fig. 2 Floor plan of overall D/A interface.

Table 1 D/A interface specification summary.

DAC	
Sampling rate	120MSample/s
Resolution	10-bit
|INL|	<0.5LSB
|DNL|	<0.5LSB
Full scale current	1mA
$Re\{\rho_G\}$	1.91e-6Ω/Ω
ρ_G	1.26e-4Ω/Ω
σ_n/I_u	<0.0126
Segmention	6+4
Current to voltage	
DC open loop gain	≥70dB
Output swing	2V (differential)
Slew rate	≥ 251.33V/μs
GBW	≥ 160MHz
Feedback resister	1kΩ

3. CIRCUIT IMPLEMENTAION

Based on the system level design of proposed D/A interface, the floor plan of overall circuit is shown in Fig. 4. The D/A interface are constructed by three main building blocks: DAC, A-DQS controller and current to voltage converter. The specification table, as shown in Table 1, is accomplished from the behavior modeling in the Matlab and SIMULIKE. Some non-ideality effects such as finite output impedance, time depending circuit noise [5] and statistic independent current source mismatch [5][6][7] are extracted from the practical current steering DAC. Besides, the finite op-amp gain bandwidth product (GBW), offset voltage, input parasitic capacitance and feedback resistors mismatch are considered in the current to voltage converter model, and the internal resistances of switches have also been modeling. Building the behavior level models can estimate the requirement and save the circuit level designing time.

3.1 Implementation of current-steering DAC

The current steering DAC architecture is a best choice due to evident cost and power consumption advantages when shouldering high speed and high resolution operation. They are intrinsically faster and more linear than the other type DAC. Fig. 5 shows the floor plan of designed segmented DAC, which consists of 4-bit binary and 6-bit unary sub-DAC. The segmented DAC is the area-efficiency method to achieve better DNL performance, especially when using 40% to 50% unary code.

The main elements of the current steering DAC are (i) current cell, (ii) switching matrix and (iii) row & column decoder. The 6-bit unary MSB (B4~B9) will distributed to row (input B4~B6) and column (input B7~B9) decoder respectively, then the decoder will drive the switch matrix which includes the SR latch, driver and the switch of the cascaded current sources. Four LSBs B0~B3 directly feed to the binary weighted current sources. Therefore, the switching signals will control the current flowing path of current sources. The DAC output is the summation of current from the binary and unary current sources.

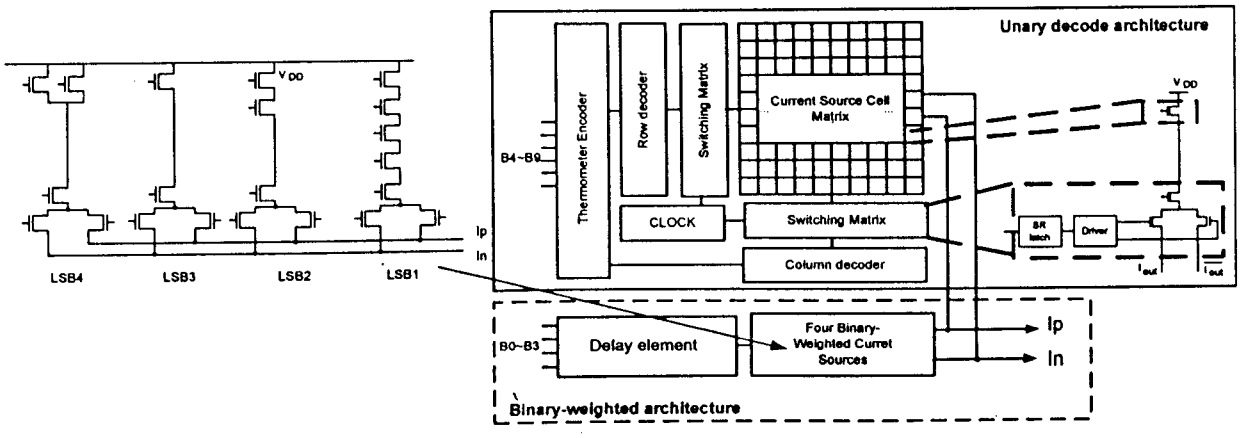

Fig. 5 Floor plan of segmented current steering DAC.

In the current cell, the output impedance will directly affect the linearity performance. The impedance observed in the output node is determined by a parallel circuit of the output resistor and a number of unity switch output impedances. The cascade configuration of the switch and current source has a sufficiently high impedance to achieve the INL and SFDR specification. Moreover, the gate overdrive voltage of current sources and area consumption are conformed to design the current cell in order to approach high yield specification.

The required accuracy on the unary current source is determined by the statistical formula [8]:

$$\frac{\sigma(I)}{I} \le \frac{1}{2C\sqrt{2^N}} \quad \text{with} \quad C = \text{inv\_norm}(0.5 + \frac{\text{yield}}{2}) \quad (1)$$

with

σ(I)/I - relative standard deviation of a unit current source;

N - resolution of the D/A converter;

inv_norm - inverse cumulative normal

yield - relative number of D/A converters with an INL<1/2 LSB

Based on the allowed relative deviation of current sources and the size versus matching relation for MOS transistor [9], the minimum dimension requirement of the unit current source can be determined.

$$(WL)_{min} = \frac{1}{2}\left[A_\beta^2 + \frac{4A_{V_T}^2}{(V_{GS}-V_T)^2}\right] \Big/ (\sigma^2(I)/I) \quad (2)$$

For the presented design, the dimensions of the unit current source transistor are given by a 10.35-μm gate-width and a 92.8-μm gate-length for a 99.7% yield specification. On the other hand, the binary weighted current sources are then built up based on the dimension of the unary current source as shown in Fig. 5.

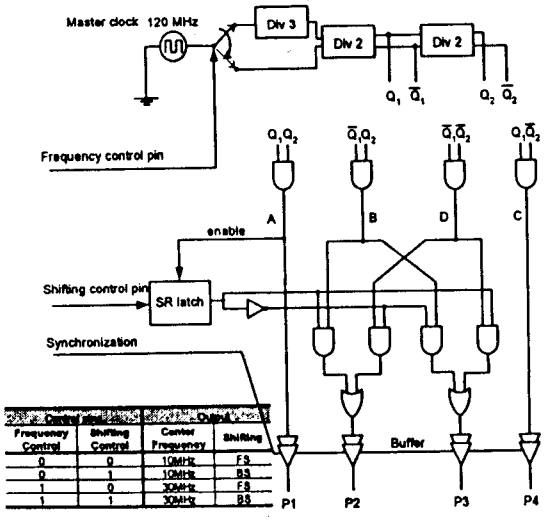

Fig. 6 Circuit diagram of A-DQS controller.

3.2 Implementation of A-DQS controller

The A-DQS controller, shown in Fig. 6, is constructed by two mainly parts: clock phase generator and frequency shifting controller. The A-DQS controller will control the baseband signal up-converted to four different intermediate frequencies. It is realized by two different oscillation frequencies modulation and FS/BS control.

The master clock with 120MHz will insert to the clock phase generator. The clock signal (10MHz or 30MHz), which frequency is controlled by the frequency control pin input, will be generating by the frequency divider. This clock signal will be operated by digital logic to generate four clock phase signal (A, B, C and D) with one fourth pulse width and same frequency as generated clock signal.

The frequency shifting controller, in fact, is arranged the phase sequence of A, B, C and D by logical operation. The arrangement of sequence is commanded by the conversion shifting. Obviously, the channel selection cannot be triggered in between the sampling sequence, thus, the channel selection is enable only at the beginning of clock phase A. The drive signal P1, P2, P3 and P4 are synchronized by the buffers.

3.3 Implementation of current to voltage converter

The current to voltage converter changes the current mode signal become voltage mode. It is required to drive next stage filter. By observing in the input node of the current to voltage converter is equivalent virtual ground, the fluctuation in the DAC output is compacted and make the generating current more stable. However, the main design challenge is the high gain and high bandwidth fully differential op-amp. In order to achieve high DC gain, the two stage op-amp with using gain and bandwidth boosting telescope amplifier in the first stage is designed as Fig. 7 [10].

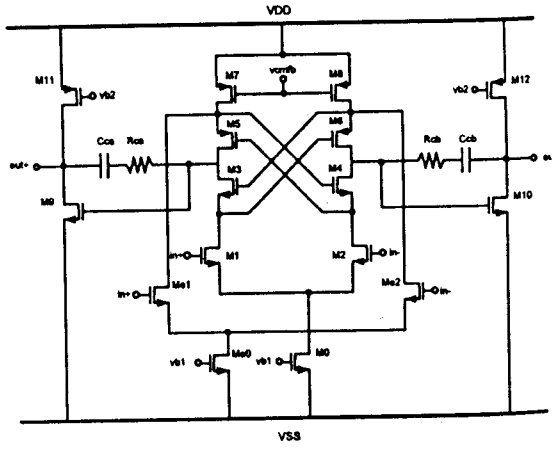

Fig. 7 Op-amp in current to voltage converter.

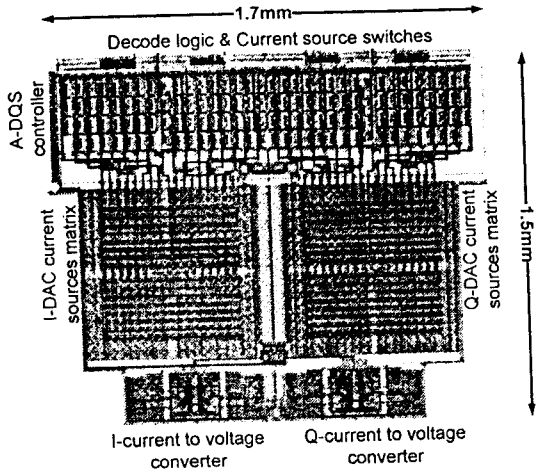

Fig. 8 Layouts of entry D/A interface.

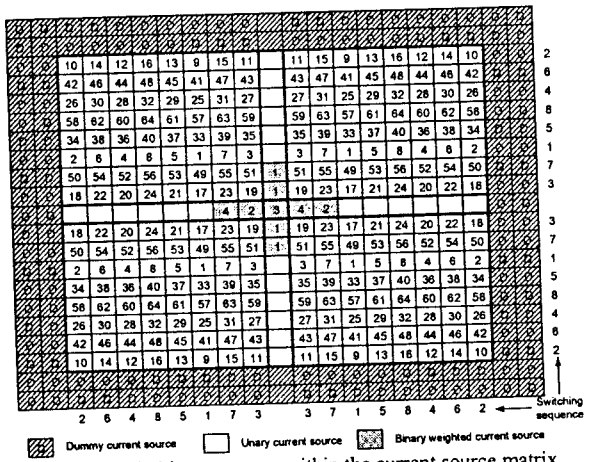

Fig. 9 The switching sequence within the current source matrix.

Proper wide-swing is employed to bias with equal I/O common mode levels at 1V for 2.5V supply, which is stabilized by improved continue time common mode feedback (CMFB) circuit.

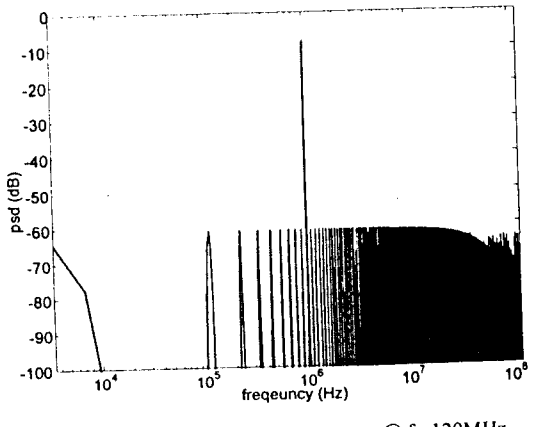

Fig.10 1MHz Sinewave spectrum @ f_s=120MHz.

3.5 Layouts

The layouts are implemented in *Cadence Virtuoso* with 0.35-μm 3-metal 2-poly CMOS. Fig. 8 shows the entry D/A interface. The substrate noise coupling and dI/dt noise are considered through careful floor planning, guard-ring and shielding in the sensitivity place as the input of current to voltage converter. Symmetric distributions are applied, especially for the current sources matrix, which static performance is sensitive to the current source mismatch. The gradient error of current source matrix is reduced by making compact matrix by separating the current source transistor, the cascaded one and switched transistor. Also, special switching scheme is applied to compensate the gradient error within the current source matrix. The INL bounded switching sequence is chosen in the row column decoding of DAC as shown in Fig. 9, since it has advantageous over other switching sequence based on typical error profile[11]. The binary weighted current source, which is shaded, is located in the center of the current source matrix (the numbered binary weighted current source indicated the LSB1, LSB2, LSB3 and LSB4). Each unary current source is separated into four units that placed in double centroid so that the spatial averaging of the error is achieved. Moreover, large arrays of matching objects exhibit proximity errors next to the gradient errors, so the dummy current source are inserted at the edge of the matrix in order to make optimal matching that the current source units see the same surroundings within a certain radius around them. The layout verifications are done with DIVA for DRC, parasitic extraction and LVS.

4. SIMULATION RESULT

The spectral purity is most important issue for the performance of the transmitter. Under the sampling frequency 120MHz of the DAC, a measured sine wave spectrum in Fig. 10 shows that the SFDR is about 56dB@1MHz. Also, the performance of D/A interface is tested in both time and frequency domain shown in Table 2.

Table 2 Performance of D/A interface.

D/A interface Performance	
Power consumption	43mW
|INL|	≤ 0.43 LSB
|DNL|	≤ 0.36 LSB
Propagation delay (rise)	4.54ns
Propagation delay (fall)	3.52ns
Settling time (rise)	12.45ns
Settling time (fall)	14.50ns
Rise time	8.6ns
Fall time	9.3ns
SFDR @ 1MHz	56.34dB

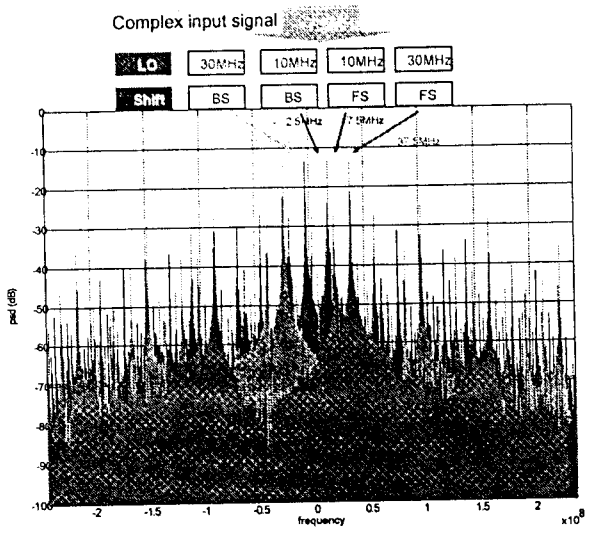

Fig.11 Functionality measured in frequency domain.

Since the proposed D/A interface is applied for wireless multistandard that focus on the maximum signal bandwidth 20MHz. To test the functionality of the D/A interface, the complex input within the range 20MHz is as its input. The tested signal is then up-converted to four different frequencies (four different channels) for different oscillations frequency and shifting scheme that are controlled by A-DQS controller. The simulation result for one of the complex test input with 7.5MHz is illustrated in Fig. 11.

5. CONCLUSION

The multistandard capability of modern wireless systems is presently in a great demand. The traditional wireless transceivers are required to improve the architecture in order to satisfy the requirements for new developments or applications. A novel transmitter architecture is presented that allows the reduction of the off-chip passive components usually encountered in traditional implementations. Moreover, a high effective two-step channel selection technique is implemented in current-mode simplifying the RF front-end frequency synthesizer settling time requirements through channel partitioning. This work will serve as a basis for the implementation of the entire two-step channel-select transmitter in the future.

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REFERENCES

[1] Paolo Orsatti, et al., "A 20-mA-Receive, 5-mA-Trnsmit, Single-Chip GSM Transceiver in 0.25-μm CMOS," *IEEE Journal of Solid-state circuits*, vol. 34, N0. 12, December 1999.

[2] D. K. Shaeffer et al., "A 115-mW 0.5-μm CMOS GPS receiver with wide dynamic-range active filters," *IEEE Journal of Solid-state circuits*, vol. 33, pp. 2219-2231, December 1998.

[3] P.-I Mak, S.-P. U and R.P Martins, "A low IF/zero-IF reconfigurable receiver with two-step channel selection technique for multistandard applications," in *Proc. of IEEE Intern. Symp. on Circuits and Systems (ISCAS)*, pp. 417-420, May 2004

[4] P.-I Mak, S.-P. U and R.P Martins, "A novel IF channel selection technique by analog-double quadrature sampling for complex low-IF receivers,," in *Proc. of Intern. Conf. on Communication Technology (ICCT)*, vol. 2, pp. 1238-1241, Apr. 2003

[5] M. Gustavsson, J.J. Wikner, and N. Tan, CMOS Data Converters for Communications, Kluwer Academic Publishers, Boston, MA, USA, Jan. 2000, ISBN 0-7923-7780-X

[6] A. Van den Bosch, et al., "A 10b 1GSample/s Nyquist Current-Steering CMOS DAC," *IEEE J. Solid-State Circuits*, vol.36, no. 3, pp.315-324, Mar. 2001

[7] C.-H. Lin and K. Bult, "A 10-b 500-MSample/s CMOS DAC in 0.6 mm ," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1948–1958, Dec. 1998.

[8] A. Van den Bosch and al., "An Accurate Statistical Yield Model for CMOS Current-Steering D/A Converters", *IEEE Intl. Symp.* Circuits and Systems, vol.4 pp. 105-108, 2000

[9] M. Pelgrom et. al., "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. SC-24, pp. 1433-1439, Oct. 1989

[10] M.M. Amourah, R.L. Geiger, "Gain and bandwidth boosting techniques for high-speed operational amplifiers," *IEEE ISCAS 2001*, vol.1, pp. 232-235, May 2001

[11] Y. Cong and R. Geiger, "Switching sequence optimization for gradient error compensation in thermometer-decoded DAC arrays," *IEEE trans. Circuit Syst. II*, vol. 47, pp. 585-595, July 2000.

[12] M. Pelgrom et al., "Matching properties of MOS transistors," *IEEE J.Solid-State Circuits*, vol. SC-24, pp. 1433–1439, Oct. 1989.

[13] J. Bastos, M. Steyaert, and W. Sansen, "A high yield 12-bit 250-MS/s CMOS D/A converter," in *Proc. IEEE 1996 Custom Integrated Circuits Conf. (CICC)*, May 1996, pp. 20.6.1–20.6.4.