A Novel Low -Voltage 2nd-Order Sigma-Delta Modulator with Double-Sampling for GSM/DECT/WCDMA

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Abstract--**This paper presents the design of a double-sampling multilevel Sigma-Delta Modulator (SDM), with relaxed opamp requirements, for GSM/DECT/WCDMA communication standards. The modulator operates with 1.8V voltage supply (with chopper stabilization technique) and has been implemented in 0.35μm CMOS. A novel dynamic element matching (DEM) technique is introduced for double-sampling SDM. The moving sum effect resulting from the fully floating switched-capacitor integrator in the feedback path has been reduced in order that the noise shaping performance remains unchanged in the signal band. The achieved SNR's are 88dB/70dB/55dB for GSM/DECT/WCDMA, respectively.**

Keywords: sigma delta, double-sampling, RDWA, moving sum,

I. INTROUDCTION

The major focus of modern RF receivers IC design has been on the increase of the adaptability and integration of multi-standard communication standards. The multi-standard ADC is the main part of the multi-standard RF receiver [1]. Sigma-delta modulators (SDM) [2] are good candidates since they don't suffer as greatly as other analog circuits from CMOS technology down-scaling and can achieve high resolution for low to medium signal bandwidth. Several SDM's for multi-standard applications have been proposed recently [1-3]. However, in [1] & [2], the SDM needs to use 4 opamps and extra digital cancellation logic circuits. Besides, some extra control circuitry is needed for multi-standard adaptability, thus increasing the circuit complexity and also the chip area and power consumption. In addition, the performance of [3] is relatively low being adequate for only two of the standards. The SDM proposed in this paper exhibits high-speed, containing a high dynamic range sigma-delta ADC for GSM/DECT/WCDMA systems. On the other hand, the integrated circuit design has been optimized to cope with low-voltage and low-power applications.

In order to minimize the system architecture and to satisfy the system requirements, a single loop 2nd order SDM structure, including a multibit quantizer, will be designed and implemented. A notable disadvantage of multibit systems is that they are not able to achieve excellent linearity without the use of precisely matched components, like in the case of single-bit systems. The integral linearity of a noise-shaping conversion system is not better than the integral linearity of the multibit internal DAC. Therefore, to achieve high integral linearity and low total harmonic distortion (THD) it is necessary to impose as a stringent requirement the need of precisely matched components. In this paper, an improved double-sampling 2nd-order SDM with an eight level quantizer is proposed. A modified dynamic weight average (DWA) technique is used to relax the matching requirements of the DAC components. In section 2, the circuit architecture will be described, followed by its integrated circuit implementation on section 3. Section 4 will present the results of simulation and finally in section 5 the conclusions will be drawn.

II. CIRCUIT ARCHITECTURE

A. Proposed Sigma Delta Modulator

The block diagram of the proposed circuit architecture is shown in Figure 1. Since the offset voltage cannot be neglected for the proposed low-pass SDM, a chopper-stabilized technique [4] is used to reduce the error. According with the requirements of 3 different communication standards [2] [3], the proposed circuit is able to achieve an adequate performance.

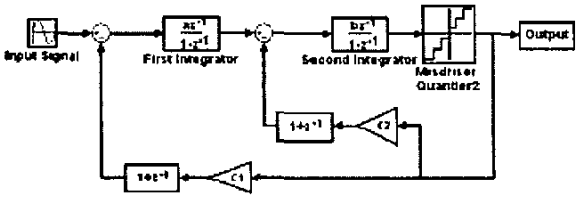

Fig. 1 Block diagram of the proposed SDM.

In order to achieve the highest performance, the circuit coefficients must be optimized. The signal and noise transfer functions, respectively (STF) and (NTF), can be expressed as equation 1 & 2:

$$STF: \frac{0.5Z^{-2}}{1-1.5Z^{-1}+1.25Z^{-2}-0.25Z^{-3}} \quad (1)$$

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$$NTF:\frac{(1-Z^{-1})^2}{1-1.5Z^{-1}+1.25Z^{-2}-0.25Z^{-3}} \quad (2)$$

with system coefficients: a = 0.5, b = 1 C_1 =0.5, C_2 =0.5.

B. Double-Sampling with reduced Moving Sum effect

In order to relax the requirements of the gain-bandwidth (GBW) of the OTA, double-sampling (DS) technique is employed, thus achieving effectively twice the sampling rate without extra requirements of the OTA settling time and dc gain. However, the DS has a drawback that imposes the need for doubling the value of the sampling capacitor, in such a way that the area is almost doubled. Besides, the capacitor mismatch in the feedback path will degrade the system performance [5]. This can be improved through the use of a fully floating switched-capacitor (SC) [5], which implements the DS without doubling the capacitor value. However, neither of the switching positions is referred to a voltage source, which will introduce a moving sum effect that imposes a term of the type $(1 + z^{-1})$ in the transfer function. This can easily create system instability that will significantly degrade the system's performance. To reduce this effect, the feedback path gain must be scaled down, leading to the lowest case of OSR (over-sampling ratio) = 16 in WCDMA, with $|1 + z^{-1}| \sim 2$. Another advantage of DS is the capacitor value of the feedback branch that can be half-scaled. Since the sampling capacitor mismatch will not cause noise in the signal band, the conventional DS can be employed in the sampling path to provide proper biasing voltage.

C. DAC with Novel Repeated-DWA (RDWA)

The DWA algorithm will implement the effective dynamic element matching (DEM) technique alleviating the matching requirements of the feedback capacitor. It provides first order noise shaping of the DAC nonlinearity together with a simple hardware structure [6]. Bi-DWA [7] can also be employed to eliminate the tones generated by the DWA algorithm. Due to the requirement of DS, double DWA generation will be necessary for both phases 1 & 2. The Bi-DWA algorithm can easily be generated by the rotation of 2 different pointers in both phases 1 & 2, respectively. In the proposed circuit, the 2 pointers rotate in the same direction (as opposite to Bi-DWA) which is designated as Repeated-DWA (RDWA). A 3 bits DAC example of RDWA is shown in Figure 2.

The simulation results shown in Figure 3 are based on the 3 bits 2 nd order SDM with OSR (64) and have 6 bits accuracy on the feedback capacitor. The mismatch of the unit elements can be modeled by the Gaussian distributed random number with mean equals to ideal value and standard derivation corresponding to the requirement of the accuracy. It is demonstrated that the SNR of the system with RDWA is slightly higher than with Bi-DWA. In addition, the hardware of the two DWA generations is the same except for the driving clock phases. Thus, it is much more attractive for design and suitable for a double-sampling application since no extra pointer and digital circuit would be required.

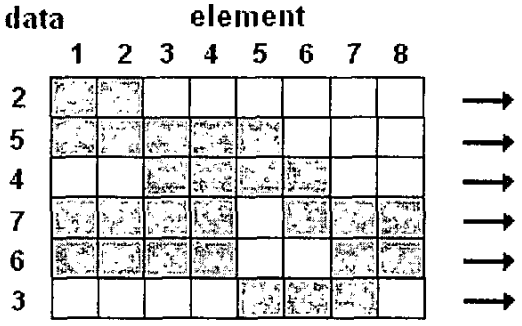


Fig. 2 Concept of RDWA (3bit DAC example)

D. SC integrator of SDM

The first SC integrator of the proposed modulator is shown in Figure 4. On the other hand, the second SC integrator has the same structure as the first one except the capacitance values that are different. Figure 5 shows the architecture of the quantizer and the digital control parts.

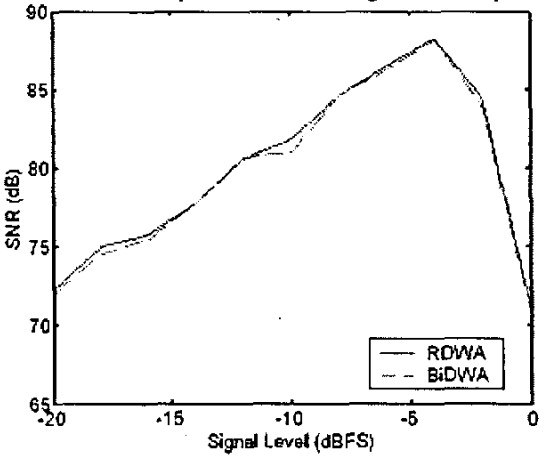


Fig. 3 Simulated SNR vs. input level for RDWA.

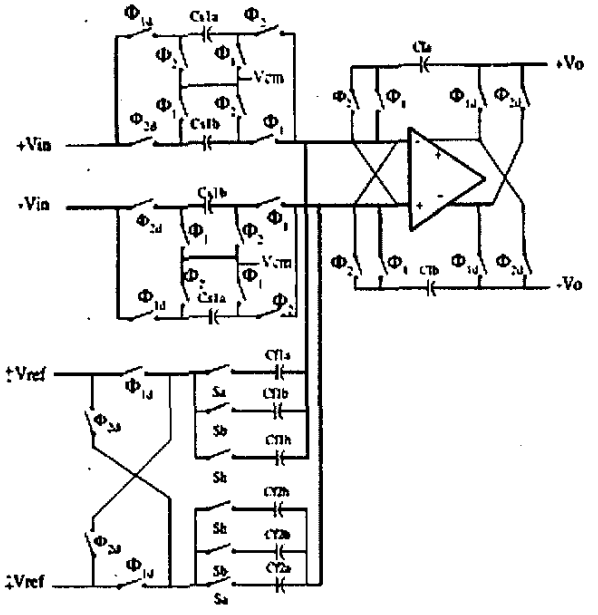


Fig. 4 First integrator of the Proposed SDM.

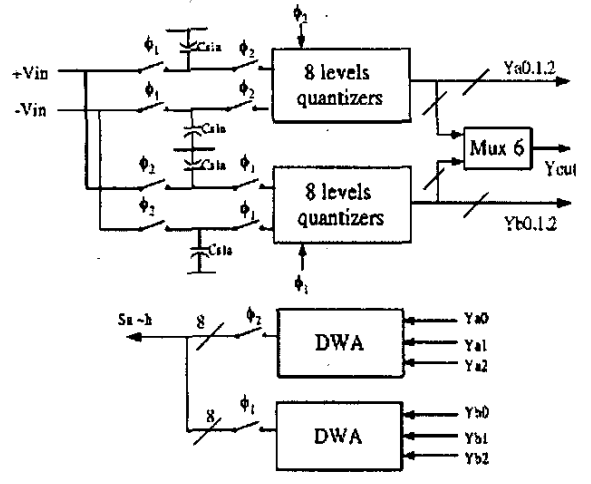


Fig. 5 Architecture of the quantizer & digital control.

III. Circuit Implementation

The proposed 2nd-order double-sampled SDM has been implemented in a 0.35-μ m double-poly, triple-metal CMOS process. The most critical part of the circuit implementation was the design of the OTA. Since the voltage supply is only 1.8V in the proposed process and the output swing required is over 1V, a 2-stages OTA with rail-to-rail output is required. In order to minimize the power consumption and maximize the gain, a telescopic architecture has been employed in the first stage amplifier. A fully-differential 2-stages OTA was then designed, with miller compensation, with the circuit architecture shown in Figure 6, and the performance results presented in Table 1.

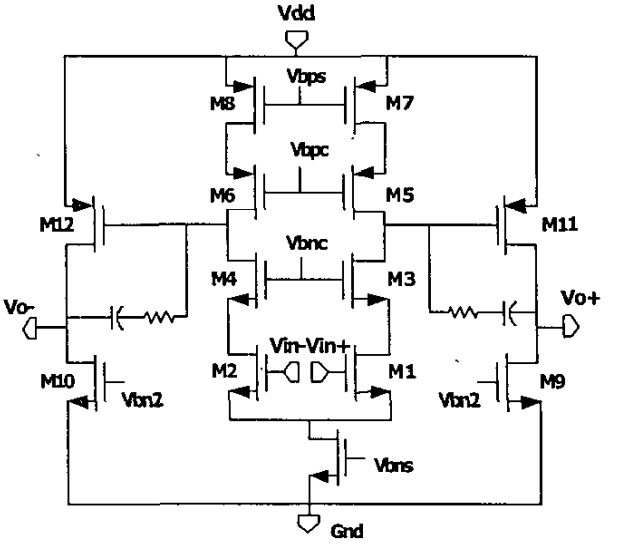


Fig. 6 Two-stages miller compensated OTA with common-mode feedback.

In a multilevel quantizer the performance of the comparator is also a critical point. Since there are 8 quantizer levels and the resolution is limited to 62mV, it will be necessary to use 16 1-bit fully-differential high resolution comparators for both clock phase 1 & 2. The basic circuit structure of the ADC with multilevel quantizer is shown in Figure 7. In which, the circuit of the comparator is shown in Figure 8. They will operate at each non-overlapping clock phase and they will latch both data through a digital latch to use as feedback. Regarding the switching of the SC integrator, the clock voltage level is not enough to drive the switches, which implies the need for a local clock bootstrapping technique that will be used to drive the switches and to ensure the appropriate linearity.

Table 1 Summary of OTA performance.

Parameters	1st stage
DC gain (open loop Gain)	98 dB
Phase Margin	51.1 Deg
Power Consumption	1.56 mW
Differential Output swing	1.45 V
Slew rate	79.1 V/us
Unity gain frequency	119.4 MHz
Input referred noise	5.8n V^2_{rms}
Capacitor Load	3.8p F

IV. Simulation Results

The proposed SDM, from Figure 4, has been characterized through a behavioral simulation in a Cadence environment. Each sampling capacitor has a value of 3.2pF in the first integrator. As an example, Figure 9 shows the comparison between the behavior of the proposed SDM model, with moving sum reduction, and the ideal model

without moving sum effect, for the WCDMA specifications. Figure 10 shows the comparison between the ideal spectrum and the proposed SDM with and without DEM. The comparison of the effect of the proposed RDWA algorithm with and without any DEM randomization under different signal level (SL) is also made, as presented in Figures 11 a) and b), for GSM specifications. Finally, in order to demonstrate that the sigma-delta modulator (SDM) can fulfill all of those 3 communication standards, the SNR vs input signal amplitude is also shown in Figure 12, being the results summarized in Table 2. The comparison of the existing SDM with the proposed one is provided in Table 3.

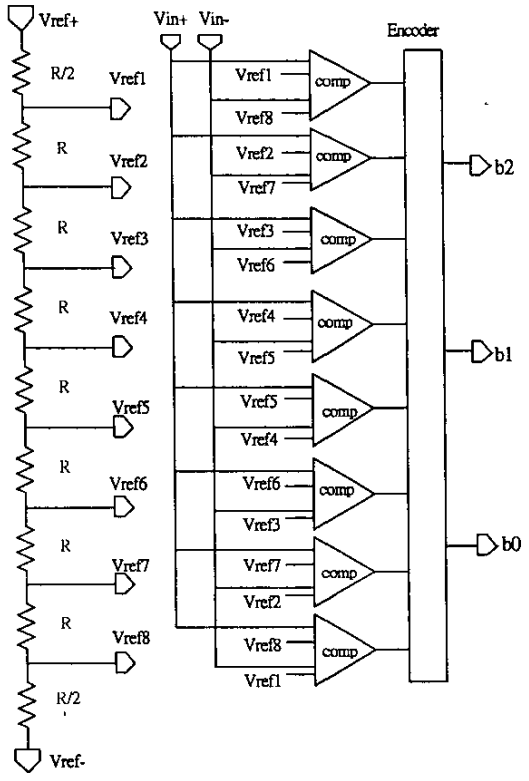


Fig. 7 The simply circuit of the 3 bits ADC

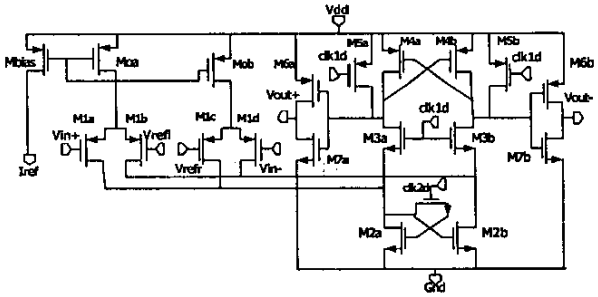


Fig. 8 The comparator circuit schematic.

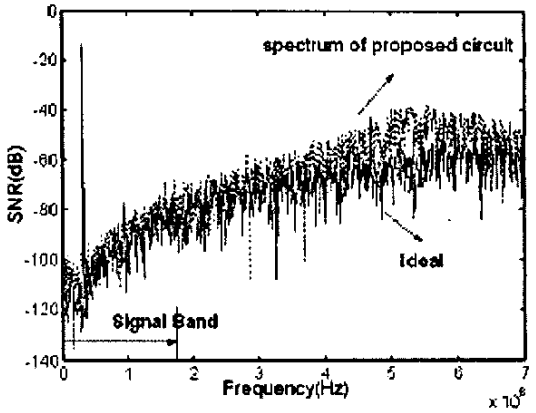


Fig. 9 Comparison between the proposed SDM with and without moving sum effect.

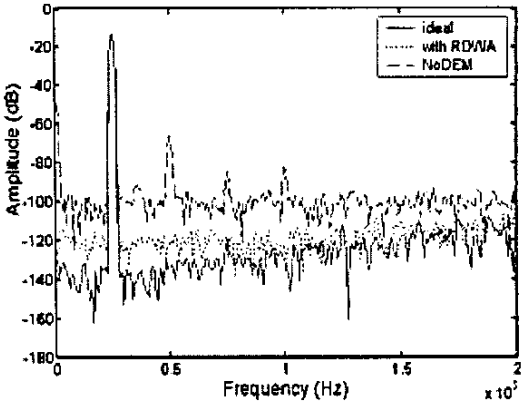
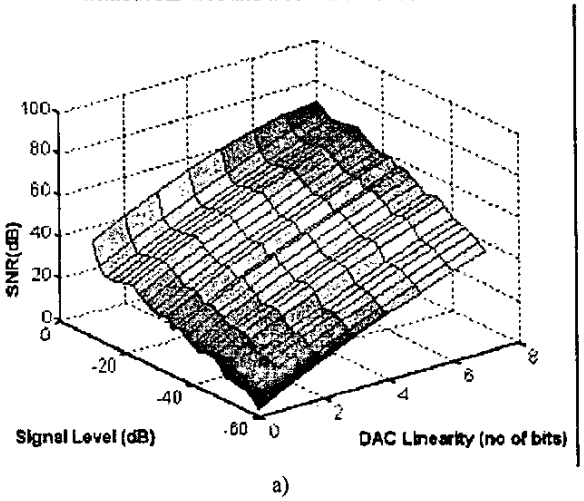
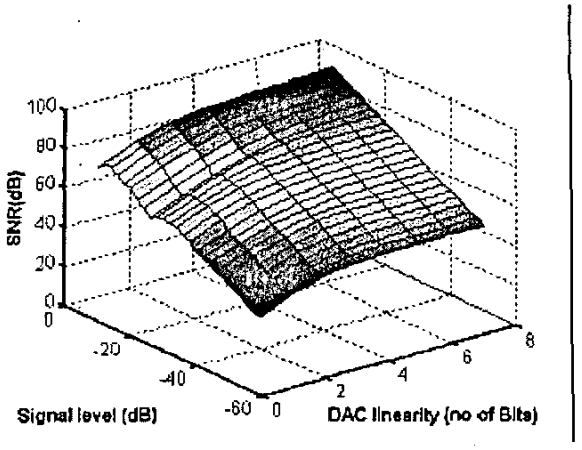


Fig. 10 Comparison between the proposed SDM with and without RDWA and also with the ideal one



a)



b)

Fig. 11 SNR vs DAC linearity for OSR = 128x without DEM (a) and with RDWA (b)

Table 2 Summary of the SDM simulation results.

	GSM	DECT	WCDMA
Signal Bandwidth	200kHz	1.4MHz	5MHz
Sampling Frequency	12.8MHz	22.4MHz	40MHz
OSR	128	32	16
DAC linearity	6bits	6bits	6bits
SNDR	88dB	70dB	55dB

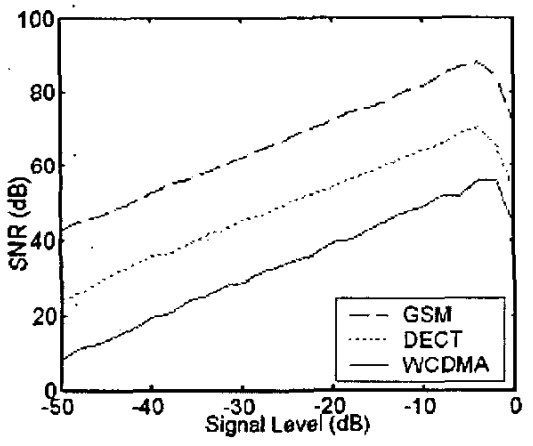


Fig. 12 The comparator circuit schematic.

Table 3 Comparison of the existing Sigma Delta Modulator

Refs	[2]	[3]	[7]	This Work
OSR	32/128	12/65	8	16/32/128
Topology	2-2	2-0	2-1-1	2-0
Bandwidth (Mhz)	0.7/0.2	2/0.2	1.25	2.5/0.7/0.2
SNDR (dB)	85/96	50/79	87	55/70/88
Process	0.35μ	0.13μ	0.5μ 5V	0.35μ
	3.3V CMOS	1.5V CMOS	CMOS	1.8V CMOS
Quantizer	1bits	5 levels	4bits	3bits

V. CONCLUSIONS

This paper proposed a robust double-sampled, chopper-stabilized, multi-level and multi-standard SDM. Simulation results have shown that it is particularly adequate to be in the presence of stringent requirements. By varying the sampling frequency through programming, this SDM can be suitably applied in the three most common communication systems, following the standards of GSM, DECT and WCDMA. Consequently, the moving sum effect is relatively small in the proposed architecture even under the smallest OSR (16), like in the case of our application. In addition, the newly proposed RDWA can effectively reduce the DAC nonlinearity within the signal band. If a comparison is made with some existing multi-standard SDM architectures the proposed modulator, not only minimizes the number of op-amps that are required, but also satisfies more demanding communication standards with higher performance and lower power consumption.

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