A Novel Semi-MASH Sub-stage for High-order Cascade Sigma-Delta Modulators

Chon-In Lao, Seng-Pan U [1] and R. P. Martins [2]

Analog and Mixed-Signal VLSI Laboratory (http://www.fst.umac.mo/lab/ans_vlsi), FST, University of Macau, Macao, China
1 – Also with Chipidea Microelectronics (Macau) Ltd., 2 – On leave from Instituto Superior Técnico/UTL, Lisbon, Portugal

***Abstract*— This paper presents a novel architecture for a high-order cascade oversampling modulator: semi-MASH (1+1-…), based on the application of stage feedback within each stage and using appropriate error cancellation logic to spread the Noise Transfer Function (NTF) zero to extend the Signal-to-Quantization Noise Ratio (SNQR). Moreover, minimum-noise-shaping-per-stage keeps 0dB overload region regardless of the stage number. An 8xOSR 5th.order 1.5-bit semi-MASH design (1+1-1+1-1mb) will be presented as an example achieving 81 dB Peak SNQR and 88 dB SFDR. More than 14 dB SNQR and 12 dB SFDR are gained by spreading the NTF zero. Behavioral simulations with MATLAB and SIMULINK demonstrate the good performance of the proposed architecture.**

I. INTRODUCTION

Modern electronic systems used in wireline and wireless communications require both high data rate and low power consumption for portable commercial products. The analog-to-digital converter is being pushed to operate at several to tens of MHz bandwidth with 10- to 16- bit resolution and low power consumption. Traditionally, Nyquist-rate ADC using pipeline technology is well suited for MHz range applications [1]. However, when resolution and linearity increase, the design headroom becomes tighter, multi-standard is necessary and cost optimization is more relevant. Pipeline technology will become insufficient and inefficient to fulfill the specification. As small oversampling ratio is always needed to relax the analog frond-end, low OSR sigma-delta technology is another technique that can be used to implement such high-resolution wide-bandwidth ADC [2].

Cascade oversampling modulator (MASH) is one of the popular low OSR sigma-delta technologies [2]. Comparing it with single-stage sigma-delta technology [3], it doesn't suffer from the unconditional stability causing large systematic SNR loss and overload region. MASH topology comprises noise-shaping and error-cancellation techniques, which leads to a greater system relaxation since the unconditional stability doesn't occur. However, traditional MASH topology suffers from several problems, namely, stage overload, noise-shaping extension (spread NTF zero) and sensitive to weight mismatch. If the first and successive stages are second-order SDM, the effect of weight mismatch will be reduced and the NTF zero can be spread, resulting in higher SNQR (Figure 1). However, more attenuation will be needed in the signal being transmitted from stage to stage to prevent the problem of overload. This will cause systematic SNQR loss and the overload point will be larger as the number of stages increases. If the successive stages are of first-order, the overload of each stage will be relaxed, but NTF zero is forced into DC and more sensitive to the weight mismatch. There exists a trade-off between the mismatch sensitive, noise-shaping extension and stage overload in traditional MASH topology.

A novel semi-MASH topology (1+1-…) will be presented in this paper that solves both stage overload and noise-shaping extension, simultaneously. It follows a new structural principle of introducing feedback within each MASH stage that has first-order noise-shaping. It merges two individual first-order MASH stages with feedback that will become an equivalent second-order noise-shaping with a pair of controllable NTF zeros. The designation of semi-MASH will stand for two stages not individualized and merged into a half-MASH structure. The notation 1+1 stands for the following meaning: two first-order noise-shaping are added together to become a second-order noise-shaping (1+1=2). This Semi-MASH topology contains two main benefits: firstly, it reduces the systematic loss by using minimize-noise-shaping-per-stage to keep 0 dB overload point regardless of the number of stages; secondly, it extends the noise-shaping by appling a feedback within each stage and using appropriate error cancellation logic to spread the NTF zero within the bandwidth. The color noise due to first-order noise-shaping will also be suppressed by the stage feedback. When compared with traditional MASH designs and their corresponding trade-offs, the proposed topology will result in a higher performance and more systematic design flow, with a higher degree of design flexibility and optimization. In Sections II and III the architecture study and simulation results will be presented and discussed. Conclusions will be drawn in Section IV.

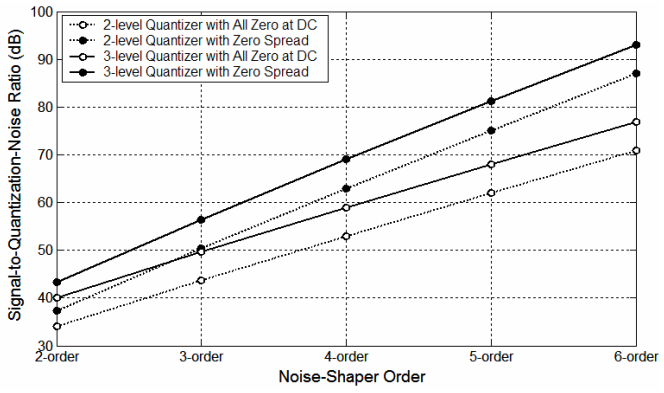

Figure 1. Peak SNQR vs. Noise-Shaper order with 8xOSR.

II. ARCHITECTURE STUDY

The proposed novel architecture of a semi-MASH sub-stage is shown in Figure 2. The analog part of a high-order sigma–delta modulator includes a chain of Semi-MASH sub-stages, each of them consisting of two first-order sigma-delta modulators. These comprise a half-delay integrator in the forward path and a half-delay in the feedback path. The minimum-noise-shaping-per-stage is used to minimize the overload region to 0dB independently of the number of stages. It results in an expandable architecture [2]. Traditionally, MASH architectures that are obtained from the combination of first-order sigma-delta modulators (1-1-…) will force all zeros to be located at DC. Moreover, the pattern noise and tone in the first stage is very large due to the usage of one-order noise-shaping. If imperfect digital cancellation occurs, the color noise and tone will leak to the final output and will imply a larger distortion. In the proposed Semi-MASH topology (1+1-…), a stage feedback path is applied to merge these two first-order SDM stages. It can spread two NTF zeros from DC by appropriate control of the feedback and using adequate error cancellation logic. On the other hand, the feedback acts as dithering for the first stage SDM to suppress the pattern noise and tone. Imperfect cancellation will only cause white noise leakage but not distortion. If perfect cancellation occurs, the signal transfer function and noise transfer function of the proposed Semi-MASH are obtained as presented in (1) ~ (3). The digital cancellation logic used to cancel the internal quantizer error can be expressed as (4) ~ (6). Where the NTF zero location is given by (7) and if N is odd, one additional NTF zero appears at DC. As shown in Figure 1, the Semi-MASH increases SNQR more efficiently than traditional MASH architecture, for example 8xOSR 5th order 1.5-bit semi-MASH has higher SNQR than an 8xOSR 6th order 1.5-bit traditional MASH structure. For example, 5th order semi-MASH digital cancellation logic is presented in (8)-(12), as well as STF, NTF, and the modulation output are determined by (13)-(15).

$$STF = G_1 \times \left(z^{-1/2} \right)^N \tag{1}$$

$$NTF_N\big|_{N\ is\ odd} = \left(1 - z^{-1}\right) \times \frac{\prod_{i=1}^{(N-1)/2} \left(1 + (G_{2i}\beta_{(2i-1)2i} - 2)z^{-1} + z^{-2}\right)}{\prod_{i=2}^{N} G_i} \tag{2}$$

$$NTF_N\big|_{N\ is\ even} = \frac{\prod_{i=1}^{N/2} \left(1 + \left(G_{2i}\beta_{(2i-1)2i} - 2\right)z^{-1} + z^{-2}\right)}{\prod_{i=2}^{N} G_i} \tag{3}$$

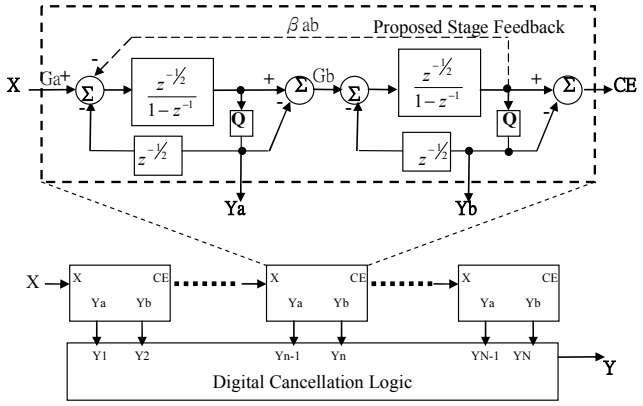

Figure 2. Block Diagram of a Semi-MASH sub-stage.

$$Hy_1 = \left(z^{-1/2} \right)^4 \tag{8}$$

$$Hy_2 = \left(z^{-1/2} \right)^3 \times \frac{1}{G_2} \times \left(1 + \left(G_2\beta_{12} - 1\right)z^{-1}\right) \tag{9}$$

$$Hy_3 = \left(z^{-1/2} \right)^2 \times \frac{\left(1 + \left(G_2\beta_{12} - 2\right)z^{-1} + z^{-2}\right)}{G_2 G_3} \tag{10}$$

$$Hy_4 = \left(z^{-1/2} \right)^1 \times \frac{\left(1 + \left(G_2\beta_{12} - 2\right)z^{-1} + z^{-2}\right)}{G_2 G_2 G_3} \times \left(1 + \left(G_4\beta_{34} - 1\right)z^{-1}\right) \tag{11}$$

$$Hy_5 = \frac{\left(1 + \left(G_2\beta_{12} - 2\right)z^{-1} + z^{-2}\right)\left(1 + \left(G_4\beta_{34} - 2\right)z^{-1} + z^{-2}\right)}{G_2 G_3 G_4 G_5} \tag{12}$$

$$STF = G_1 \times \left(z^{-1/2} \right)^5 \tag{13}$$

$$NTF_5 = \left(1 - z^{-1}\right) \times \frac{\left(1 + \left(G_2\beta_{12} - 2\right)z^{-1} + z^{-2}\right)\left(1 + \left(G_4\beta_{34} - 2\right)z^{-1} + z^{-2}\right)}{G_2 G_3 G_4 G_5} \tag{14}$$

$$Y = X \times STF + E_5 \times NTF_5 \tag{15}$$

$$Hy_n\big|_{n\ is\ odd} = \left(z^{-1/2} \right)^{(N-n)} \times \frac{\prod_{i=1}^{(n-1)/2} \left(1 + \left(G_{2i}\beta_{(2i-1)2i} - 2\right)z^{-1} + z^{-2}\right)}{\prod_{i=2}^{n} G_i} \tag{4}$$

$$Hy_n\big|_{n\ is\ even} = \left(z^{-1/2} \right)^{(N-n)} \times \frac{\prod_{i=1}^{n/2-1} \left(1 + (G_{2i}\beta_{(2i-1)2i} - 2)z^{-1} + z^{-2}\right)}{\prod_{i=2}^{n} G_i} \times \left(1 + \left(G_n\beta_{(n-1)n} - 1\right)z^{-1}\right) \tag{5}$$

$$Y = \sum_{i=1}^{N} \left(H_i \times Y_i\right) = X \times STF + E_N \times NTF_N \tag{6}$$

$$f\theta_i = \pm \frac{fs}{2\pi} \cos^{-1}\left(1 - \frac{G_{2i}\beta_{(2i-1)2i}}{2}\right) \quad for \quad i = 1 \sim floor\left(\frac{N}{2}\right) \tag{7}$$

III. Simulation Results and Analysis

Behavior simulations have been done in MATLAB and SIMULINK to verify the novel proposed architecture, using 8x OSR and 1.5-bit internal quantizer. The input level is normalized to the quantizer full swing which minimizes the quantization error. The sampling frequency is normalized to 1 and bandwidth to 0.0625. In Figure 3, the plus marker stands for MASH 1-1-… from 2 to 6 numbers of stages and circle marker stands for Semi-MASH 1+1-… from 2 to 6 numbers of stages. The proposed Semi-MASH is more efficient increasing SNQR when compared with the traditional architecture. The overload point occurs after 0 dB for both architectures due to the use of minimum-noise-shaping-per-stage.

An 8xOSR 1.5-bit 5^{th}-order cascade SDM will be explored as a design example. Figure 4 shows the in-band output PSD and SNQR from MASH 1-1-1-1-1 with input signal level swept. All zeros are forced to be located at DC and the peak SNQR is 67dB whereas the peak SFDR is 76dB. Figure 5 shows the in-band output PSD and SNQR from Semi-MASH 1+1-1+1-1 with input signal level swept. The NTF zero is spread equally within the signal bandwidth and results in lower noise floor. The peak SNQR is 81dB and the peak SFDR is 88dB. More than 14dB SNQR and DR, and 12dB SFDR is gained from the Semi-MASH architecture. The proposed semi-Mash will not suffer form the stability problem. As shown in Figure 1, the SNQR of a 5^{th} order 1.5-bit semi-MASH is higher than a 6^{th} order 1.5-bit MASH. The proposed Semi-MASH architecture reduces one stage and increases power efficiency. We can sweep the NTF zero location to get the optimized NTF zero location. Figure 6 shows the contour plot of SNQR vs. two pair of NTF zero location that is controlled by the stage feedback coefficient β. Since this is a 5^{th} order modulator, one zero is located at DC. As shown in Figure 6, the contour plot is symmetrical and the maximum SNQR occurs at the NTF zero near equally spread. When we have the NTF zero location, we can get the value of the stage feedback coefficient β using (7).

Figure 7 shows the effect of finite DC gain, where high DC gain is needed to avoid the SNQR drop due to the integrator leakage. Various techniques have been proposed to have gain compensation for switched-capacitor integrators [4, 5]. The weight mismatch of the stage feedback will only cause variation of the NTF zero. However, imperfect cancellation of the internal quantizer error between each substage causes large SNQR drop. Figure 8 shows the effect of weight mismatch with 30 Monte-Carlo simulations before calibration. To overcome the problem, we can combine semi-MASH 1+1-1+1-…and MASH 2-1-1-…[2], i.e., 2-1+1-…. Another solution will use the calibration technique [6, 7]. Figure 9 shows the effect of weight mismatch with 30 Monte-Carlo simulations if the calibration that matches the digital coefficient to analog coefficient is performed.

The proposed topology introduces a new idea to extend the SNQR by merging two stages with a feedback. The new idea of stage feedback can be extended to other existing sigma-delta topologies such as bandpass, complex, parallel and continuous cascade single/multi-bit SDM to achieve an optimum design.

IV. Conclusions

In this paper a new topology that applies feedback between two individual sigma-delta modulators from a MASH architecture is presented. The proposed Semi-MASH sub-stage (1+1-1+1-…) extends SNQR, DR and SFDR, improving the overload region. The NTF zero can be controlled by this stage feedback and appropriate digital cancellation logic. The overload region is also improved to 0dB by using minimum-noise-shaping-per-stage. However, the proposed topologies suffer from circuit non-idealities such as finite DC gain and weight mismatch. Specific compensation and calibration techniques are necessary to be applied to overcome these issues. The proposed topology can be combined with existing cascade sigma-delta topologies in order that an optimum design could be achieved.

Acknowledgment

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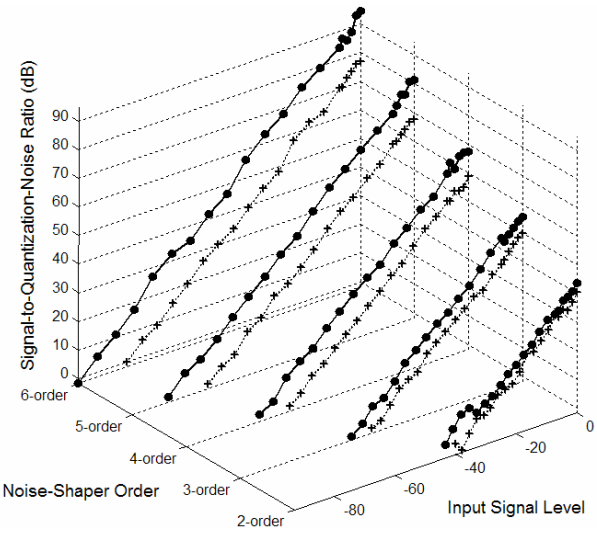

Figure 3. SNQR vs. Input Signal Level plot: Plus Marker: all NTF zero at DC; Circle Marker: NTF zero spread equally.

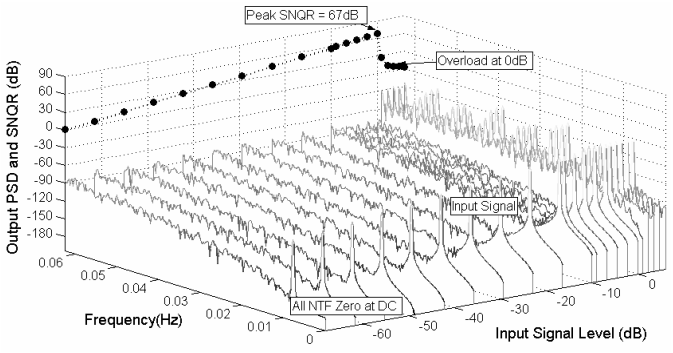

Figure 4. In-band Output PSD and SNQR vs. Input Signal Level with all five NTF zero locate at DC.

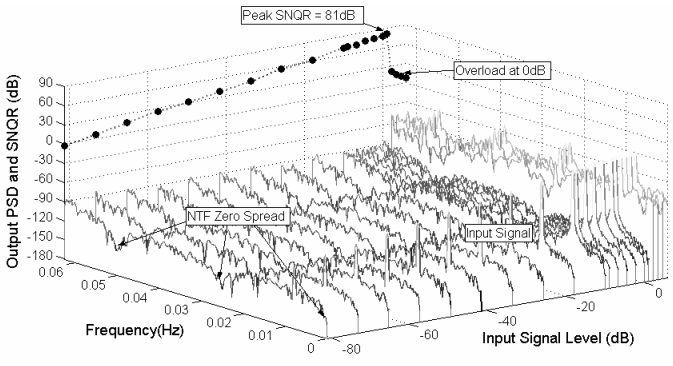

Figure 5. In-band Output PSD and SNQR vs. Input Signal Level with five NTF zero equally spread within the bandwidth.

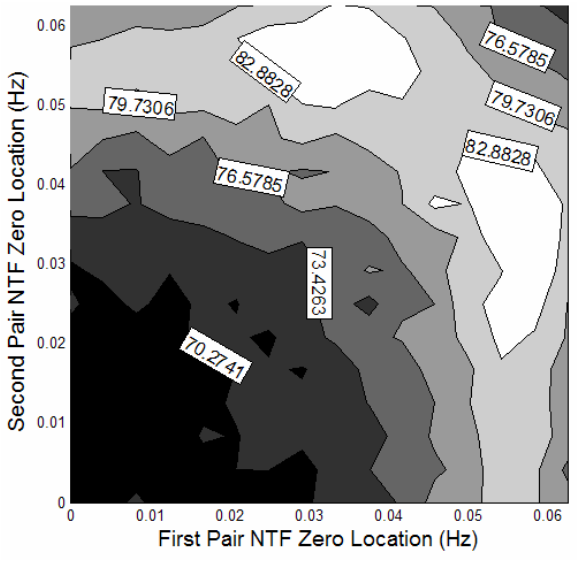

Figure 6. SNQR vs. NTF Zero Location (Contour Plot).

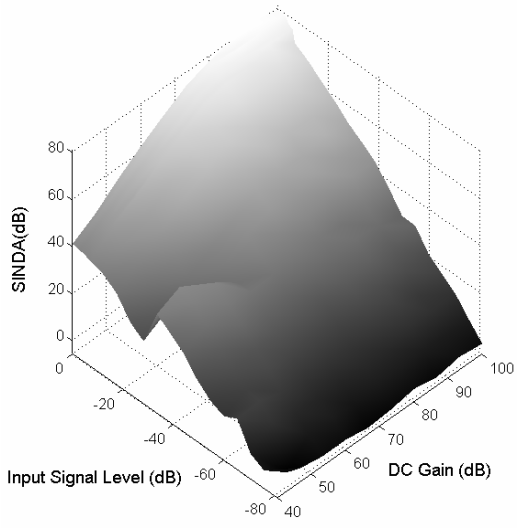

Figure 7. SNQR vs. DC gain.

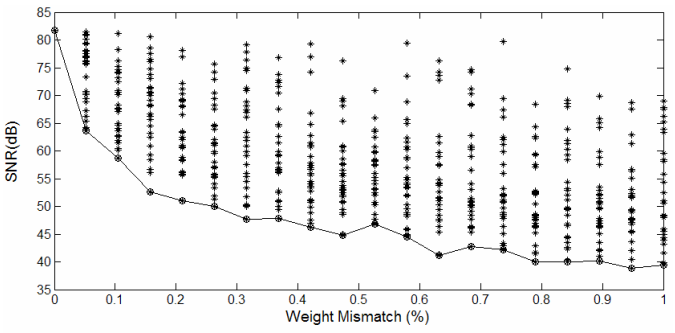

Figure 8. SNQR vs. Weight Mismatch (Before Calibration).

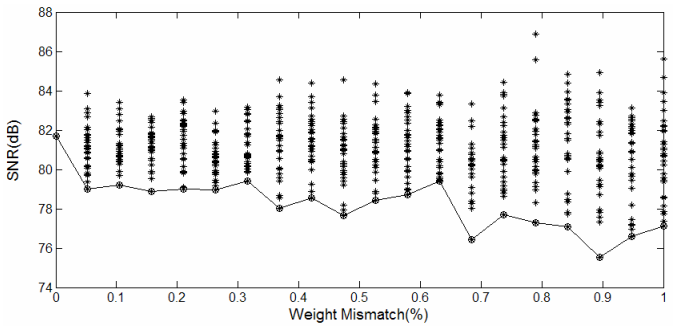

Figure 9. SNQR vs. Weight Mismatch (After Calibration).

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