A Power-and-Area Efficient, Multifunctional CMOS A/D Interface for a Low-IF/ Zero-IF Reconfigurable Receiver

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ABSTRACT

A multifunctional CMOS analog-to-digital (A/D) interface was designed for a low-IF/zero-IF reconfigurable receiver. Such an interface combined IF-mixing, channel-selection, and *I/Q*-multiplexing techniques to minimize both the area and power. The overall interface achieved 7.7-b ENOB, along with INL and DNL within ±0.5LSB and ±0.34LSB, respectively. The chip area is 1.34mm^2, while dissipating 54.5mW for digitization both *I* and *Q* channels.

1. INTRODUCTION

Power and area minimizations of wireless transceiver ICs are imperative to reduce both the battery size and manufacturing cost of portable devices. In designing multistandard receiver analog front-ends (AFEs) that satisfy modern communication standards requirements, a low-IF/zero-IF reconfigurable architecture emerged as a highly flexible topology than their individual [1]. Their advantageous features can be joined by employing two-step-channel-selection (2-SCS) technique [2]. Such an improved architecture, as shown in Fig. 1, not only reduces the phase-locked loop frequency synthesizer (PLL-FS) phase noise and settling time requirements through channel selection partitioning from the RF AFE to the IF interface, but also allows simple digital reconfigurations.

This paper presents an implementation of such receiver baseband circuitry, which includes a sample-and-hold (S/H) pair embedding Analog-Double Quadrature Sampling (A-DQS) [3], combined with an *I/Q*-multiplexing pipelined A/D core [4]. These techniques efficiently join the functionalities of IF-to-baseband down-conversion, second step of channel selection, and single-ADC-*I/Q*-digitization in one chain. Thus, the occupied chip area and power consumption can be highly compressed. Another vital advantage is the elimination of *I/Q* imbalance in the A/D conversion, with the correspondent improvements in image rejection.

The targeted applications of this receiver are the 2.4-GHz standards including Bluetooth, IEEE 802.11FH and HomeRF, since the power consumption is a major concern, and demanding low phase noise and fast settling time requirements of the PLL-FS, which needs to perform frequency-hopping continuously.

2. RECEIVER ARCHITECTURE

2.1 Overview

Designing both low-power and high-performance multistandard wireless receiver chip-set involves plenty of design issues, especially the cost-efficiency and industrial-worth of the

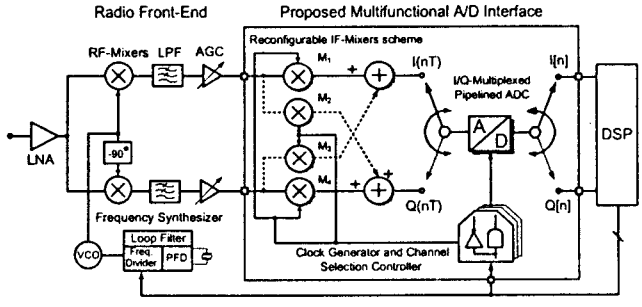


Fig. 1 Low-IF/zero-IF reconfigurable receiver architecture.

applications. Since all Bluetooth, IEEE 802.11FH and HomeRF standards operate in the same 2.4-GHz industrial-scientific-medical (ISM) band and features many resemblances in their physical (PHY) layer specifications [5], only one antenna and transceiver AFE are needed to satisfy both transmit and receive operations. Moreover, those standards specify different data rates and operation distances for personal-, home- to office-applications, they are therefore not appearing to be substitutable to each other.

2.2 Frequency planning in low-IF mode

The main novelty exhibits in the proposed receiver is an enhanced two-step channel-selection (2-SCS) technique. Figure 2(a)-(d) shows the hierarchical spectra-flow illustrations of the proposed frequency planning with the selected IF equal to half-channel spacing, i.e. 500 kHz, for both Bluetooth and IEEE 802.11FH applications. Similar to general approaches in the radio-platform for frequency-division multiple-access (FDMA) wireless standards, the pre-selected channels, $x_{RF}(t)$, (arbitrarily labeled as C_N and C_{N+1} for $N=1,2,3$) will be amplified by a low noise amplifier (LNA) first. Second, assuming that the targeted radio channels are C_N and C_{N+1}, (the first step of 2-SCS)

$$x_{RF}(t) = C_N \cos[2\pi f_N t + \phi_N(t)] + C_{N+1}\cos[2\pi f_{N+1} t + \phi_{N+1}(t)] + C_{N+2}\cdots \quad (1)$$

where C_N, f_N and φ_N are the constant envelope, frequency and phase of channel N, respectively. After lower sideband quadrature downconversion, channel C_N will be the corresponding image interferer of channel C_{N+1} or vice versa. In other words, dual-channel is downconverted together to the identical IF, but with conjugate complex representations. It is noteworthy that if this dual-channel is distinguishable in the IF, the possible local oscillator (LO) frequency f_{LO} will be simplified from 1 to 2 channels bandwidth, and its locking positions are halved. This free dual-channel downconversion is the fundamental characteristic of quadrature receiver with the main difference is

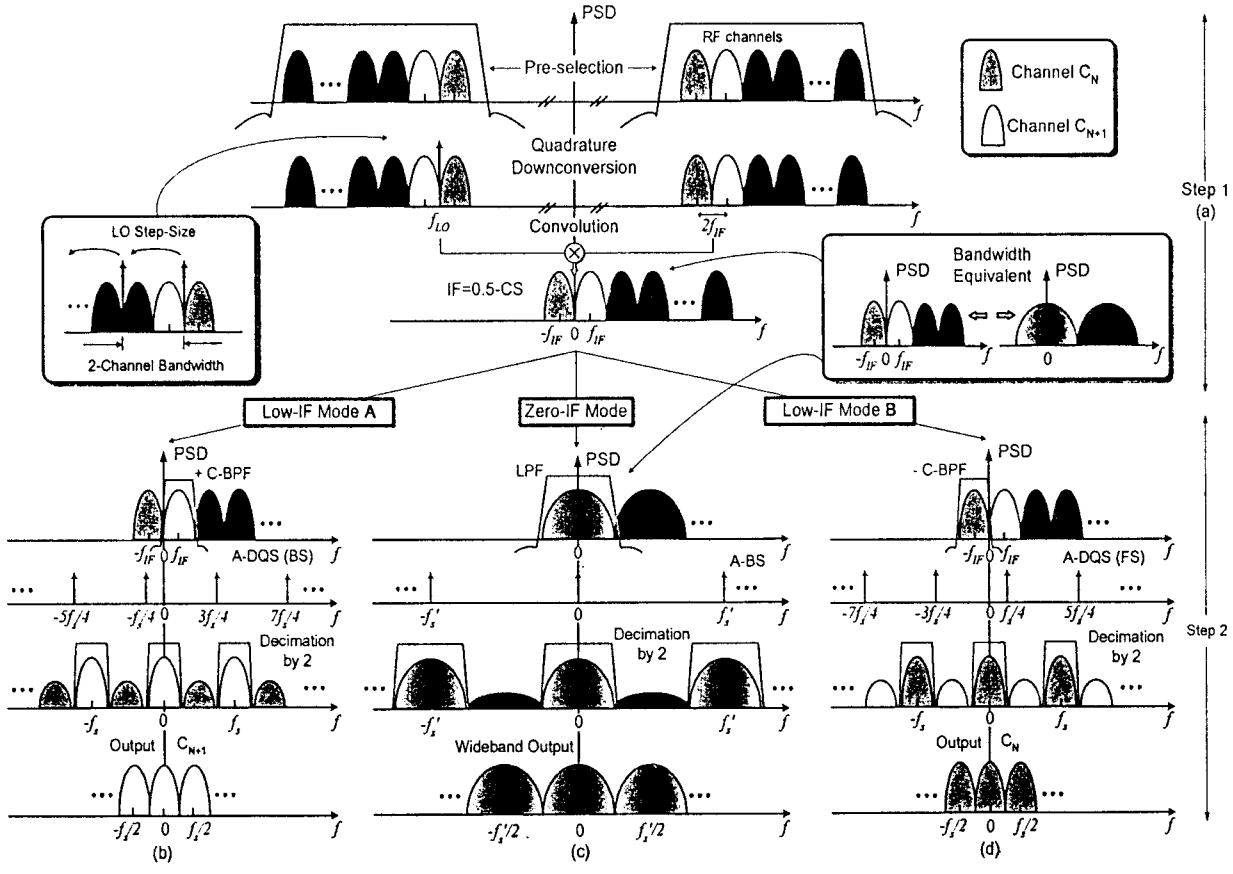


Fig. 2 CSSF illustrations of receiver showed in Fig. 1. (a) Step-1: RF AFE. (b) Step-2: low-IF mode-A. (c) Step-2: zero-IF. (d) Step-2: low-IF mode-B.

the concept of image interferer, which is now considered as the adjacent channel of the desired one. Then, the minimum step-size of the RF PLL-FS, also the required reference frequency, can be extended from 1MHz to 2 MHz to exhibit better spectral purity. In addition, the values of the modulus in the PLL-FS can be halved. Referring to the typical design equations of the widely-used type-II *integer-N* PLL-FS [6], halves the modulus values significantly lowers both the close-in phase noise and locking time of the PLL-FS by 50%, while the out-of-band phase noise is reduced by a factor of $\sqrt{2}$. Furthermore, this also extends the PLL-FS phase margin in some extent to improve its stability. The cost for such improvements is a second step of channel selection that needed in the IF-downconverter as described as follows. After proper amplification and filtering by lowpass or polyphase bandpass filter, channel C_N (located at $-f_{IF}$) and C_{N+1} (located at f_{IF}) will face a programmable analog-double quadrature sampling (A-DQS) that will result in an either backward (BS) or forward (FS) frequency shifting. This double quadrature sampling technique intrinsically offers both sampling and frequency down-conversion when the sampling frequency is set to 4 times the IF, whilst offering the flexibility that it can be control to acquire either the upper- or lower-sideband. As a result, after the A-DQS operation, the complex-IF signals are equivalently to be multiplied by a controllable complex term, $cos(n\pi/2)\pm jsin(n\pi/2)$ for $n=0,1,2,...$The positive sign in this term is the FS, i.e. channel C_N is obtained at $\pm nf_s$ for $n=0, 1, 2...$whereas channel C_{N+1} (image of C_N) is shifted to $\pm nf_s/2$ for $n=1, 3, 5...$ Similar results could be obtained for BS with the considerations put on the negative sign, then the role of channel C_N and C_{N+1} are reversed. This simple polarity changing can be easily accomplished through differential circuit implementation. Both cases do not suffer from the problematic DC-offset and flicker noise since they are now shifted to $\pm nf_s/4$, for $n=1, 3, 5....$ Then, for the first-time in the literature, by exploring the consecutive-code independent property of pipelined A/D converter, single A/D converter can be employed to digitize both *I*- and *Q*-channels by means of *I/Q*-multiplexing. Therefore, the area and power consumptions, as well as *I/Q*-mismatch in the A/D converter are significantly reduced. The final *I*- and *Q*-data at a rate $f_s/2$ can be obtained after digital filtering and decimation by a factor of two. The other baseband functions include the demodulation, equalization and mode selection can be implemented in the digital signal processor (DSP) to achieve the greatest flexibility.

2.3 Zero-IF mode

Another constructive consequence of such 2-SCS technique explored in this work is that when two narrowband channels are considered as a wideband one as [Fig. 2], the LO frequency will be selected on the same frequency as the channels' carrier to directly downconvert it to the baseband (i.e., a zero-IF operation). One may argue that two narrowband channels' bandwidth (BW) may not be exactly equal to the BW of one single wideband

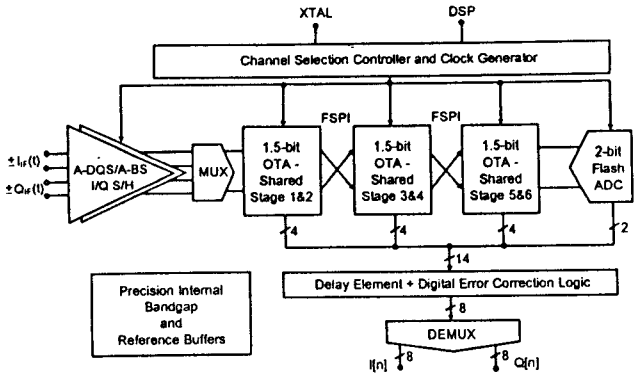


Fig. 3 Detailed architecture of the proposed A/D interface.

channel. However, the cost is only a BW tunable low-Q filter and it is just a common practice in design multistandard systems. The A-DQS will be replaced by its sub-set analog-baseband sampling (A-BS) by considering the mixers M_2 and M_3 in Fig. 1 are null (i.e., no quadrature phase samplings) and increases the f_s to 10 MHz to match the HomeRF channel spacing and reduce the aliasing. The subsequent operations are analogous to those in low-IF mode.

3. IMPLEMENTATION

3.1 Anatomy of the A/D interface

According to the aforementioned operations, the differences between low- and zero-IF operations are predominantly rely on the baseband platform, which is implemented in this work by exploiting the proposed A/D interface based on an 8-bit 20-MHz pipelined A/D core architecture as illustrated in Fig. 3. The front-end sample-and-holds (S/Hs) are the A-DQS/A-BS scheme that will perform the sampling, IF-to-baseband downconversion and IF channel selection through simple digital control in low-IF mode, or just A-BS one in zero-IF mode. The sampled I/Q -signal will be time-interleavely inputted into the pipelined A/D core

Table 1. Valid design specifications.

Resolution		8 bits
A-DQS/A-BS sampling rate		10-MHz
ADC sampling rate		20-MHz
Input signal swing (differentially)		$1V_{pk\text{-}to\text{-}pk}$
Reference voltage (differentially)		0.5V
Sampling / feedback capacitor value		0.5pF
Clock duty cycle		0.4-0.6
Clock rise/fall time		<1ns
Image-rejection ratio (IRR)		>40dB
Power dissipation at 2.5V supply		Minimize
Circuit Non-idealities		
OTA	DC gain	>80dB
	Slew rate	>100V/μs
	Unity gain frequency	>180MHz
	Offset voltage	<5mV
	Noise power	<-70dB
	Input parasitic capacitance	<0.3pF
Mismatch in sample & feedback caps.		<0.5%
Capacitor top plate parasitic		<10%
Voltage reference noise		< -40dB
1.5-bit flash comparator offset voltage		<31.25mV
2-bit flash comparator offset voltage		<5mV

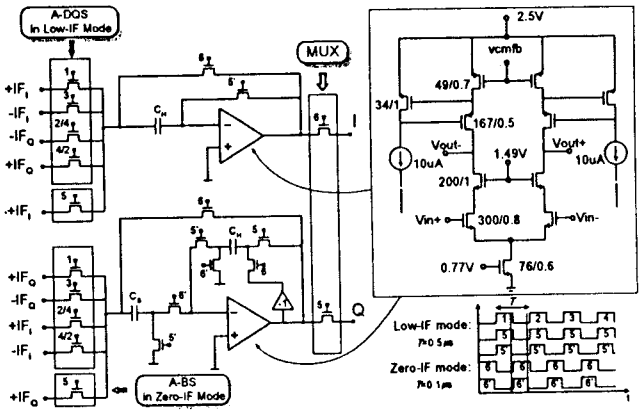


Fig. 4 A-DQS/A-BS S/H pair and MUX (simplified).

through an analog-multiplexer (MUX). The six sub-ADCs are 1.5-bit resolution stages with the operational transconductance amplifiers (OTAs) shared between two consecutive ones. The feedback signal polarity inverting (FSPI) technique is applied to reduce two-thirds of the offset voltage [7]. Other functional blocks include a 2-bit flash ADC, a bandgap current and voltage references with multi-stage driving buffer, a programmable clock phase generator, a digital error correction (DEC) logic and a digital-demultiplexer (DEMUX).

Designed in a top-down methodology, the entire system model is first emulates in *Matlab* and *Simulink* environments through our self-developed non-ideal models [8]. The deliberated circuit imperfections include the OTA non-idealities, capacitor mismatches, image-rejection due to I/Q imbalance, thermal noises, and distortion due to unstable voltage reference, etc. The final iterated design specifications are summarized in Table 1.

3.2 A-DQS/A-BS scheme and MUX

Figure 3 shows the single-ended circuit architecture of the A-DQS/A-BS scheme, which is embedded in the S/H pair of the pipelined core (the actual implementation is fully-differential). The I-channel S/H is a half-delay offset-compensated S/H, whereas the Q-channel one is a new proposed full-delay S/H with polarity inverting in each phase-change to provide offset-cancellation. This half- plus full-delay S/H pair is appropriately designed for the subsequent pipeline core to process the time-interleaved I/Q-data with only doubling of its operation frequency. It is notable that the charge-transfer in the Q-channel S/H will result a large mismatch with the I-channel one due to their diverse topologies. However, such kind of mismatch results only unproblematic self-image problem [9] since the desired signal is already settled at baseband after either A-DQS or A-BS operation. The analog-multiplexer (MUX), as shown in Fig. 4 also, can be simply implemented by four analog switches (differentially) controlled by two non-overlapping clock phases, thus, resulting insignificant influence to the entire system performance. All the switches are implemented with transmission gates (TGs) due to their front-end positions to minimize the distortion due to input-dependent charge-injection and ON-resistance variation. The implemented OTAs are gain-boosted telescopic with switched-capacitor (SC) common-mode feedback (CMFB). The open-loop gain and unity gain bandwidth (GBW) of the OTAs are approximate 88.6 dB and 207 MHz, respectively. Both the

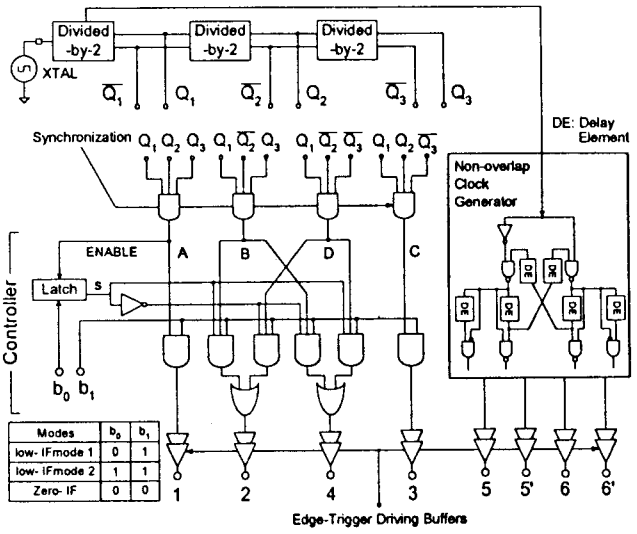


Fig. 5 Channel selection embedded clock generator.

channel and mode selections are performed by a 2-bit digital controller [Fig. 5], which is efficiently embedded in the clock phase generator. The sequential clock phases *1-4* are generated via three *divided-by-2* JK-flip-flops and simple logical operations. This approach is simple in structure and also eliminates the different propagation delays experienced in the dividers as they are synchronized in the four AND-operations to obtain phases *A* to *D*, which are then passed to the channel selection controller to switch-ON/OFF by the 2-bit control code, and performs sampling sequence (*1-2-3-4/ 1-4-3-2*) rearrangement to realize the aforesaid controllable complex term (sub-section 2.2). To ensure the channel selection is in the desired order, it is enabled with phase *A* through a latch. This also implies the time needed for one channel switching is four sampling periods. In the proposed applications, $2\mu s$ is required for 2-MHz sampling frequency (4 times the IF), which is only 1% of the time for the fastest channel switching standard Bluetooth ($200\mu s$). The phases *5* and *6*, and their early switched-off versions *5* and *6*, are the general non-overlap clocks for bottom-plate sampling in SC circuits. Specific edge trigger buffers for last-stage rising-edge synchronization are used in the driving clock to control the random process mismatches and minimize the time-skew and clock-jitter effects [10]. Moreover, since the downconversion and channel selection only acts in the control paths in discrete-time domain, the imposed transient effects on the sampled signals are neglectable. Those benefits do not exist in traditional continuous-time implementation methods.

3.3 Pipelined A/D Core

With the A-DQS/A-BS scheme also serves as the front-end S/H and MUX of the pipelined A/D core. The sub- and flash-ADCs will perform the digitization directly. The OTAs are shared within two consecutive sub-ADCs with the FSPI technique to minimize the chip-area, power-consumption, and reduce two-thirds of the offset voltage due to differential imbalances. The OTA architecture in the S/H is also utilized for each sub-ADC to save design time. Since digital error correction logic is employed in the back-end to correct the decision errors in the comparators, which are therefore design in simple resistor divider comparators with set-reset (SR) latches to further compress the power consumption. The digital back-end is shown in Fig. 6. The thermometer codes produced from the sub- and flash-ADCs are re-coded into binary

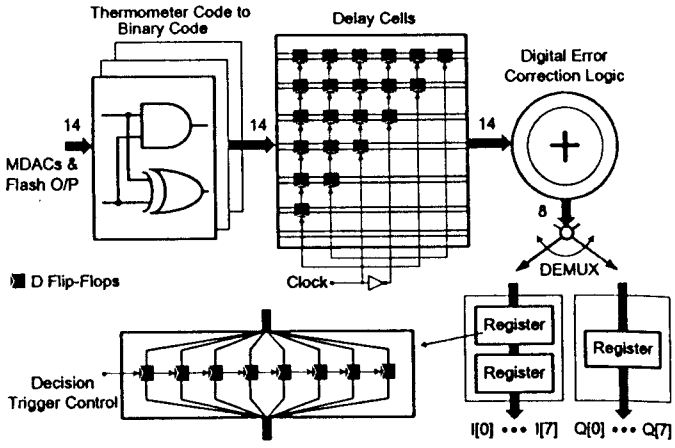


Fig. 6 Digital back-end of the pipelined A/D core.

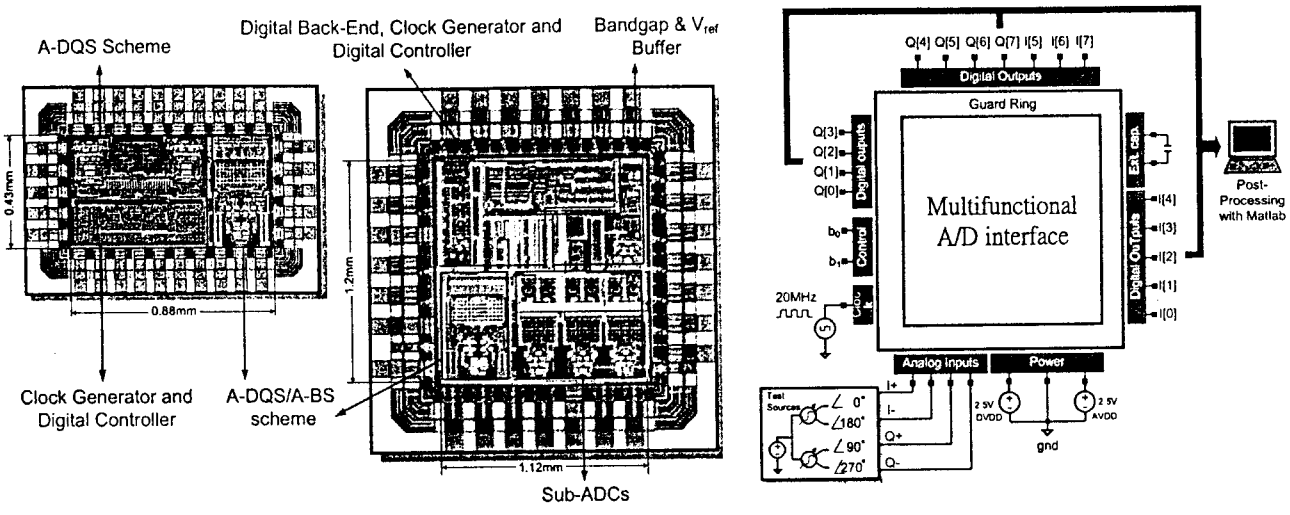
ones through simple logic operations, and then the code will be passed to the delay cells implemented by D-flip-flops (DFF) for code-synchronization. The 14-bit output codes are corrected to the final valid 8-bit codes through the digital error correction logic. Since the *I*- and *Q*-data must be synchronized in the final outputs, another three sets of delay elements implemented by DFF and simple digital control are used as the DEMUX to delay the first-outputted *I*-channel data 1 more cycle than the *Q*-channel one.

3.4 Bandgap current and voltage references

Bandgap references are employed to support both current and voltage sources to the entire A/D interface. Summing the currents generated from two current generators, one with positive and one with negative proportional to absolute temperature (PTAT) coefficient, to produce a temperature-independent current reference. Then, each individual stable current can be obtained from the current steering circuits. The common-mode voltage is generated by utilizing simple resistor string with voltage followers for buffering. For the high-precision required reference voltage, a high-performance and low-power three-stage buffer with external stabilization capacitor is utilized. The two preamps are designed to have low-gain but wideband, while the last-stage is a high-tranconductance OTA for driving the resistive feedback and minimizing the output impedance,

3.5 Layouts

The layouts are implemented in *Cadence Virtuoso* with $0.35\text{-}\mu m$ 3-metal 2-poly CMOS. Figure 7(a) shows the layout implementation of the standalone A-DQS scheme without *I/Q*-multiplexing [11] and the first-proposed A-DQS/A-BS scheme for performance comparisons. Figure 7(b) shows the entire A/D interface. The layout verifications are done with DIVA for DRC, parasitic extraction and LVS. The substrate noise coupling and *dI/dt* noise are considered through careful floor planning, double guard-ring isolation of noise-sensitive parts, multidimensional shielding and individual analog and digital power supplies with shared ground to minimize the inductivity in their current return paths for signal transferring. Ample substrate contacts and symmetrical traces routing are utilized as many as possible throughout the functional blocks interconnects, power-lines and padframes. The matching in the differential paths is maximized through common-centriod, biasing network sharing and dummy-periphery layout geometry. Special attentions are put in the *I/Q*-



(a) (b) (c)

Fig. 7 Layouts of (a) Standalone A-DQS and A-DQS/AB-S schemes. (b) Entire A/D interface and (c) its virtual testbench.

S/Hs layout, in which the *I*- and *Q*-OTAs are combined to enhance the matching accuracy whilst reducing the occupied area.

4. SIMULATION RESULTS AND TESTS

4.1 A-DQS/A-BS scheme

The performances of standalone A-DQS scheme are reported in [11] and they are omitted here. Base on the layout showed in Fig. 7(a), a parasitic-extracted simulation of the A-DQS/A-BS scheme is performed. Also for simplicity, only the operation in low-IF mode for forward frequency shifting (as mentioned in sub-section 2.2) will be shown. The simulated FFT of *I*-channel output is shown in Fig. 8(a) with a 1-MHz single tone sampled by 10MHz (*Q*-channel output is not shown as its spectrums have only phase differences with the *I*-channel ones). In complex-signal perspective, such input can be considered as one positive and one negative 1-MHz tones in the two-sided spectrum. Thus, after sampled-and-held by the A-DQS, the 1-MHz input signal is shifted by 2.5MHz ($f_s/4$) and will be located at *±n1.5MHz, ±n3.5MHz, ±n6.5MHz and ±n8.5MHz* for *n=1, 2, 3* The attenuations in their magnitudes is due to the *sin x/x* response of the S/H circuit. For the complex FFT|*I*+*jQ*| as shown in Fig. 8(b), those signals at *±n6.5MHz* and *±n8.5MHz* for *n=1, 2, 3* are cancelled since the original phase differences between those tones are in quadrature. The simulated *image-rejection ratios* (IRRs) are 41 dB, 50 dB, 76 dB for 2 % gain, 0.5° phase and 2 % capacitor mismatches, respectively. The power dissipation of this functional block is approximate 500 μW with active area of 0.17 mm^2.

4.2 Pipelined A/D Core

A virtual testbench of the A/D interface, as depicted in Fig. 7(c), is established for post-layout verifications in *Cadence Schematic Composer* environment. Due to the complex nature of the A-DQS output, the pipelined A/D core is only characterized with a 2.3-MHz single tone sampled by 10-MHz in zero-IF mode by exploiting analog-baseband sampling (A-BS), the obtained FFT results and determined performances are summarized in Fig. 9. For the static performance, the maximum *integral non-linearity* (INL) and *differential non-linearity* (DNL) are within ±0.5LSB and ±0.34LSB, respectively as shown in Fig. 10. The current reference achieves a temperature coefficient of 1.33 nA/°C and less than ±0.25μA (±2.5% of the full-scale) for a ±10% change of supply voltage. The power dissipation of the entire chip is approximate 49.5mW for digitizing both *I*- and *Q*-channels.

4.3 Test plan

Post-fabrication verifications will be carried through our in-house instruments. In addition to the entire A/D interface, the A-DQS scheme without the *I/Q*-multiplexing technique, and the A-DQS/A-BS scheme will be fabricated individually to allow performance comparisons and *I/Q*-mismatch identifications in analog-domain [Fig. 7(a)]. By injecting two quadrature phase single tones into the *I*- and *Q*-channels of the scheme, the *I/Q*-mismatch can be determined by maintaining the *I*-channel input unchanged first, and adjusts both the amplitude and phase of the *Q*-channel one until the fundamental image tone, which is online measuring by an *Anritsu MS2661C* spectrum analyzer, merges in the noise floor. Then, the corresponding IRR can be directly calculated from the measured amplitude and phase errors. The speed-test of channel selection is done by applying a 10-MHz clock on the control pins b_0 while keeping b_1 in high status [Fig. 5], and then the cyclic relocations of the test sources as shown in the output spectrum can be monitored to measure the periodicity and simultaneously verifies the functionality.

The performances indicative metrics [Fig. 9] of the entire A/D interface will be determined in zero-IF mode by applying two differential single tones into the *I*- and *Q*-channels yielding from an *Agilent* E4436B signal generator, the outputs codes are then gathered by an *Agilent* 16702B logic analyzer for data acquisition, and subsequently put in a *Matlab* installed workstation for signal diagnosis. Statistical measurements of the achievable resolutions and dynamic ranges with different sampling rates and in different prototypes will be carried to determine the performances means. The power dissipation will be measured in both standby and active modes for digital and analog parts to clarify the actual power distributions.

5. CONCLUSIONS

As the multistandard capability and power consumption of modern wireless systems are equally imperative, the standalone operation of either low- or zero-IF receiver will no longer be

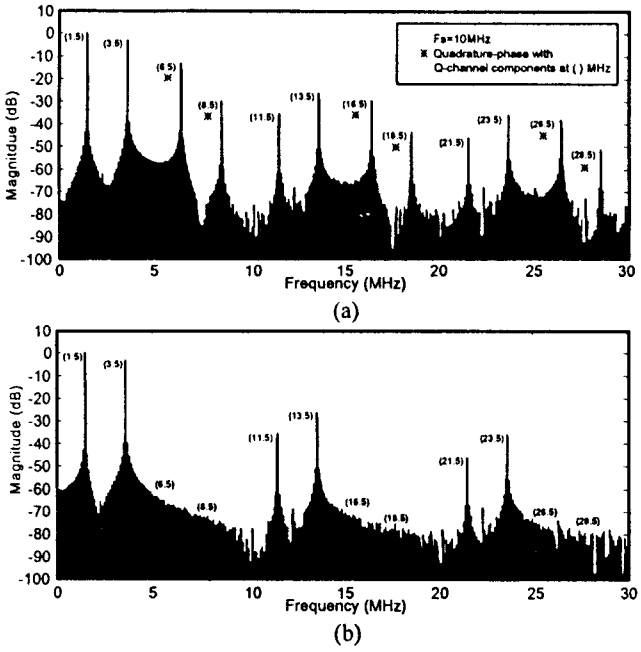


Fig. 8 FFT results of the A-DQS (a) *I*-channel. (b) $|I+jQ|$.

adequate and power efficient enough to handle both narrowband and wideband applications. This paper revealed an innovative frequency planning to combine low- and zero-IF receivers together through the proposed multifunctional A/D interface. As a result, without the need of alteration in the radio front-end, both narrow-band and wideband signals can be processed flexibly in their preferred low- and zero-IF operating modes, respectively. Such an interface features the channel-selection functionality to simplify the front-end frequency synthesizer design difficulties, and at the same time minimizes the power and area consumptions by means of both double quadrature sampling mixing and *I/Q*-multiplexing. The power and area are therefore compressed to 54.5 mW and 1.34 mm^2, respectively, for digitizing both *I* and *Q* channels.

6. ACKNOWLEDGMENTS

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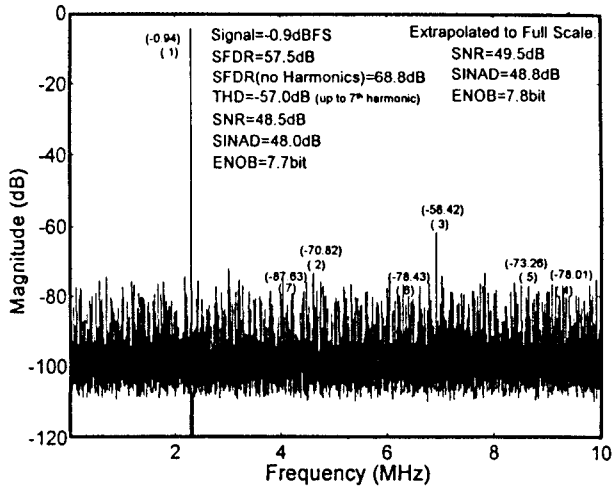

Fig. 9 FFT results the pipelined A/D core in zero-IF mode.

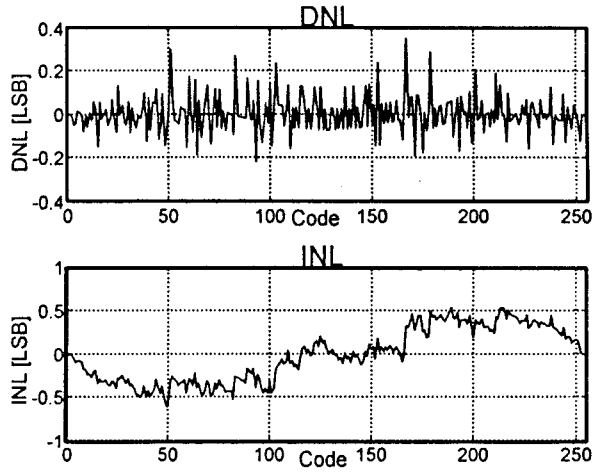

Fig. 10 DNL and INL of the pipelined A/D core.