A Robust 3rd Order Low-Distortion Multi-bit Sigma-Delta Modulator with Reduced Number of Op-amps for WCDMA

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Abstract **- This paper describes a novel single-loop multi-bit (3 bits) sigma-delta modulator (SDM) with reduced number of op-amps for wideband WCDMA. Such architecture is based in a simplified analog structure that not only features low distortion but also provides an aggressive and significantly enlarged noise shaping bandwidth with low over-sampling ratio (OSR). With a sampling frequency of 39MHz and an OSR of 10 the proposed circuit can achieve 74dB SFDR.**

I. INTRODUCTION

Oversampled sigma-delta analog-to-digital converters (sigma-delta ADCs) are well known for their capability to achieve high-resolution in low-to-medium speed applications. However, extending these converters to broadband applications requires lowering the oversampling ratio (OSR) in order to implement the sigma-delta modulator within the technology limits and reasonable values of consumable power. Due to the need of high-speed communications, the bandwidth of such modulators has been increasing up to the MHz range in recent years. High-order modulator structures and multi-bit quantizers are often used to decrease the OSR requirements without lowering their performance [1-2].

Another advantage of multi-bit quantization includes enhanced modulator stability as well as relaxed slew-rate and settling-time requirements of the operation amplifiers (opamps) in the loop-filter integrators. At low oversampling ratios (for example, 4 or 8) as required in such applications, these ADCs are increasingly sensitive to circuit imperfections [3]. Distortion components, produced by nonlinear opamp gain and limited slew-rate, are not adequately attenuated by the sigma-delta loop, which implies a careful opamp design to avoid these effects. However, there are design trade-offs to be achieved combining, simultaneously, the appropriate circuit requirements and the necessary power consumption. Opamps consume most of the power in sigma-delta ADCs, specially the first stage opamp, because of its requirements in terms of DC gain, unity-gain frequency and slew rate. The SDM proposed in this paper exhibits high-speed and low distortion, containing a high dynamic range sigma-delta ADC for WCDMA applications. In section 2, the circuit architecture will be described, followed by its integrated circuit implementation on section 3. Section 4 will present the results of simulation and finally in Section 5 the conclusions will be drawn.

II. MODULATOR DESIGN

2.1 Proposed Sigma-Delta Modulator (SDM)

To avoid the noise leakage of the uncancelled quantization noise and the digital cancellation logic, a single loop topology has been chosen instead of a cascade topology. The block diagram of the traditional architecture with multi-bit feedback is shown in Figure 1. This architecture has several drawbacks in a high-order SDM design because a high coefficient spread is required to stabilize the circuit, which not only leads to more area and power consumption, but also implies higher coefficient sensitivity and poor stability.

A low-distortion topology [3] has many advantages over the conventional structure. According with the requirements of WCDMA communication standards, different circuit topologies have been proposed [4-6] that are able to achieve an adequate performance.

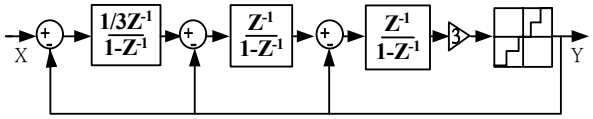

Figure 1: Traditional 3rd order SDM with distributed feedback.

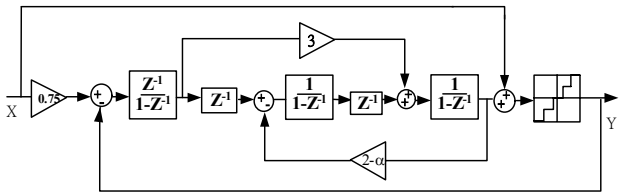

Figure 2: Generic Low Distortion SDM architecture.

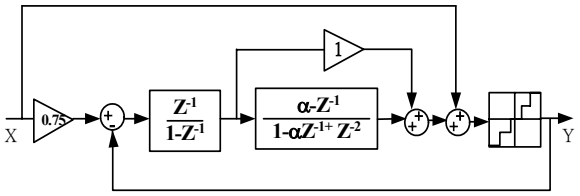

Figure 3: Proposed Architecture.

$$STF = 1 \quad (1)$$

$$NTF = (1 - Z^{-1})(1 - \alpha Z^{-1} + Z^{-2}) \quad (2)$$

Figure 2 shows a generic low distortion SDM [7] with the corresponding signal and noise transfer functions given by (1) and (2). Only one DAC in the feedback path turns the implementation more convenient especially if the calibration is used for its linearization. In fact, the second and third integrator can be shared to further decrease the power and chip area. In order to simplify the structure and reduce the redundant components, a modified circuit is proposed in figure 3. Here, the second and third opamps are grouped together to realize a second order integrator [8] and the power consumption can be reduced. Instead of placing the entire zero at DC, the modified structure spreads the zero of the second & third integrator such that a more regressive NTF can be achieved. After optimizing the circuit by simulation, the highest performance is obtained by setting α = 1.9. In the generic architecture, the feedback path 2-α is needed to spread the zeros. However, it requires very good matching of the capacitance when α is close to 2, which is not realistic. This additional feedback path is not necessary in the newly proposed architecture. With OSR= 10, a 3-bits quantizer and α = 1.9, Figure 4 shows the comparison among the SNDR of traditional, generic and the proposed structures. The simulation shows that the proposed has SNDR degradation until the input amplitude reaches -3dB, which is better than the circuit without low-distortion topology. In addition, the proposed structure achieves maximum SNDR of 64dB, which is 1dB higher than the generic circuit and 4dB higher than the traditional circuit.

2.2 Switched-Capacitor (SC) Circuit

The first integrator is similar to the conventional SC integrator with multi-bit feedback. Due to the low distortion topology, the analogy requirement of the op-amp such as the DC gain, GBW and SR can be relaxed. The second integrator and the corresponding timing diagram are shown in Figure 5. The inverting unity-gain can be implemented easily by using v_o- or v_o+ in the fully-differential configuration. One drawback of this circuit is the increasing of the capacitor loading in the second integrator, which is caused by extra-circuitry. However, the analog nonlinearity of the second amplifier will not be increased significantly due to the noise-shaping characteristic of the second integrator.

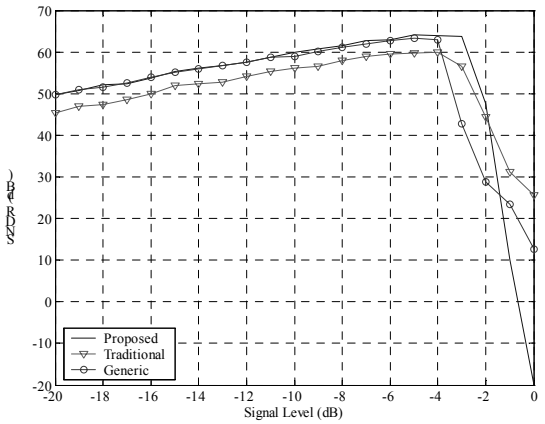

Figure 4: SNDR versus input amplitude.

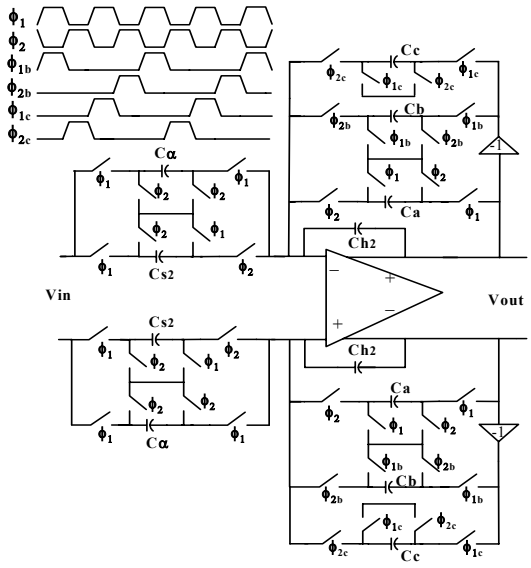

Figure 5: The circuit of the second integrator.

III OTA CIRCUIT IMPLEMENTATION

The most critical part of the circuit implementation was the design of the OTA. Since the voltage supply is only 1.8V in the proposed process, a 2-stage OTA with rail-to-rail output is required to optimize the output swing.

In order to minimize the power consumption, a class AB push-pull second stage is used to allow a low static current and achieve high slew rate. A fully-differential 2-stage OTA with 70dB gain and 120MHz unity-gain bandwidth (GBW) was designed, with Miller compensation, with the circuit architecture shown in Figure 6. In addition, eight 1-bit fully-differential comparators with 62mV of resolution were designed to implement the 3-bits quantizer. Besides, a Data Weighted Averaging (DWA) technique has been used to shape the DAC nonlinearity caused by mismatch of the feedback capacitor. The signal dependent tones will not degrade the performance of the converter since the quantization noise will be the dominant noise source in the system.

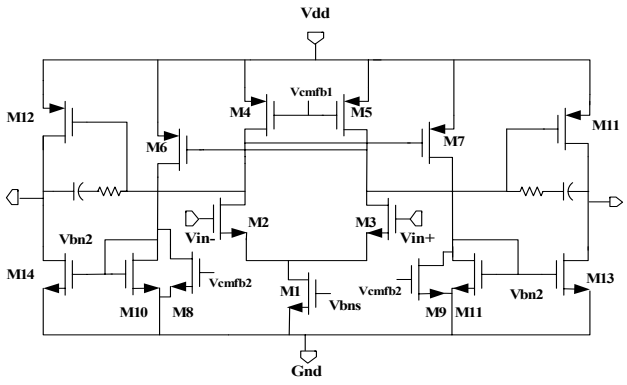

Figure 6: A 2-stage fully-differential Class AB OTA.

IV SIMULATION RESULTS

The behavioral simulation of the proposed SDM from Figure 7 was performed with the circuit parameters mentioned previously and with a sampling frequency of 39MHz with an OSR=10. Each sampling capacitor has a value of 1.6pF in the first integrator. The variation of the design parameter α due to process variations will affect the overall circuit performance. The mismatch of the unit elements has also been analyzed by using a Gaussian distribution with a mean equal to the nominal value and standard derivation corresponding to the requirement of the accuracy. With 7-bits accuracy of the unit capacitance, Figure 8 shows the statistical histogram of the 300-run simulation for SNDR. In addition, Figure 9 shows the output spectrum for an input signal frequency of 0.5MHz with $0.6V_{pp}$. The achieved SNDR/SFDR are 64dB/74dB, respectively. The results satisfy the ADC requirement for WCDMA [4~6]. Besides, the effect of the DAC nonlinearity on the SNDR under different Signal-Level (SL) is presented in Figure 10. It shows that at least 7 bits accuracy for the feedback capacitor ratio is required without significantly degrading the performance. In addition, a comparison of the existing SDMs for WCDMA with the novel proposed architecture is provided in Table 1, where it is shown that the proposed architecture obtains similar levels of accuracy when compared with others but with a simplified architecture.

V CONCLUSIONS

This paper has proposed a robust 3rd order low-distortion and opamp-reduced multi-level SDM. Simulation results have shown that the proposed SDM is particularly adequate for wideband applications such as WCDMA. Moreover, the architecture can be extended to higher order to increase the SNDR for wider signal bandwidth. Comparing the proposed SDM with existing topologies targeted for WCDMA, the proposed modulator not only reduces the number of opamps, but also satisfies more demanding communication standards with higher performance showing that this architecture is well-suited for low-power applications. Besides, chip area will also decrease with the reduction of the number of opamps.

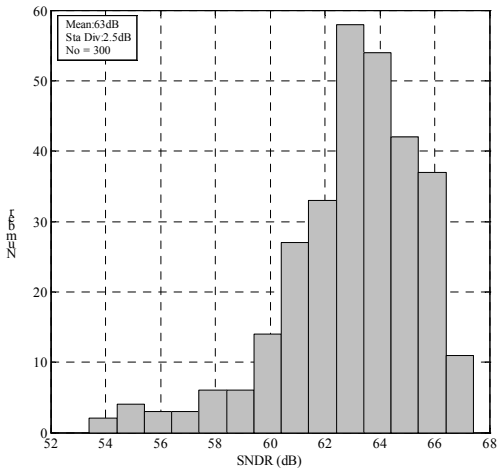

Figure 8: Histogram of 300-run Monte-Carlo simulation with capacitance variation for SNDR.

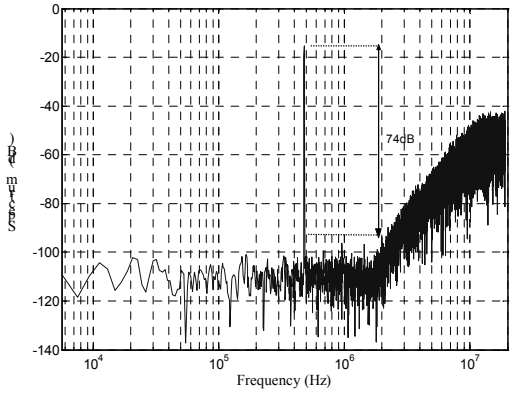

Figure 9: Output Spectrum of the Proposed SDM.

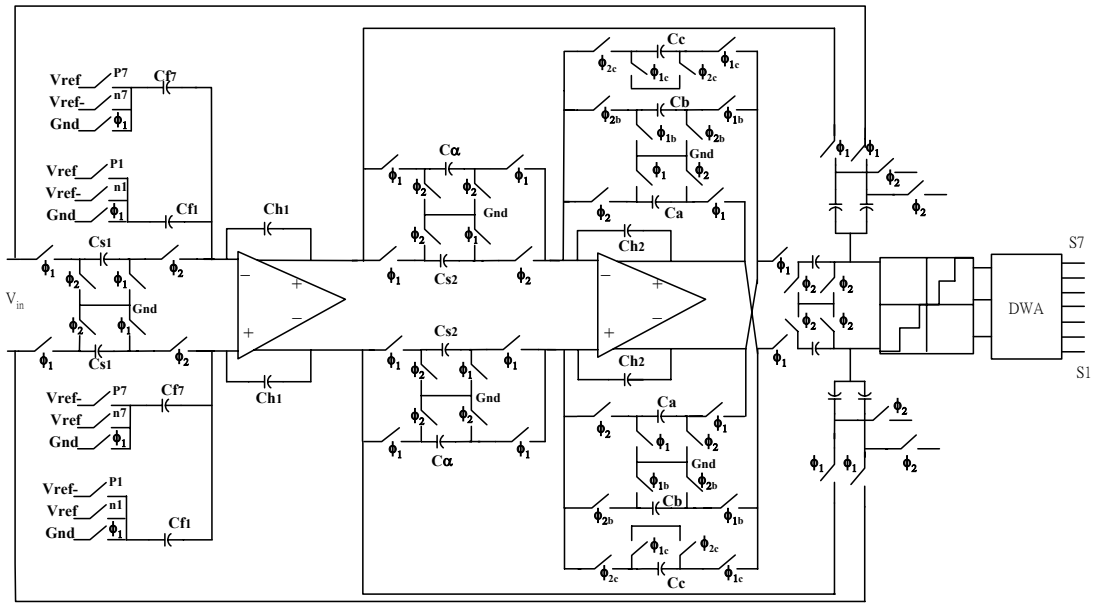

Figure 7: Circuit implementation of the proposed SDM.

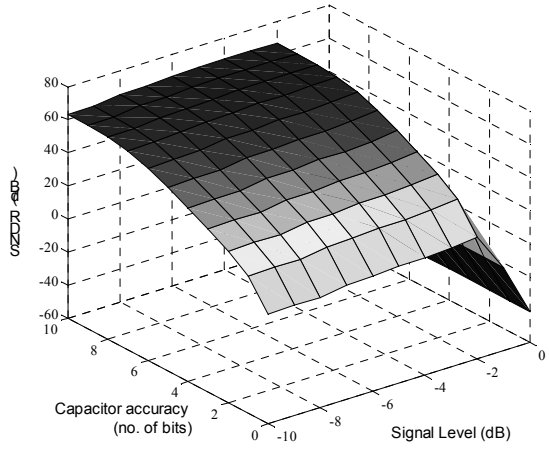

Figure 10: SNR vs DAC linearity for OSR = 10.

Table 1: Comparison among different Sigma Delta Modulators. (Ci-jBm: cascaded i-j converter where m denotes the number of bits in the quantizers. SnBm denotes n^{th}-order SDM with a m-bit quantizer.)

Refs	[4]	[5]	[6]	Proposed
OSR	10	12	8	10
Topology	C21B5	S2B2.3	C23B4	S2B3
Bandwidth (MHz)	1.92	2	1.92	1.92
SNDR (dB)	64	50	72	64

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