DESIGN AND ANALYSIS OF LOW TIMING-SKEW CLOCK GENERATION FOR TIME-INTERLEAVED SAMPLED-DATA SYSTEMS

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ABSTRACT

This paper will first analyze the output phase-skew effects with embedding the practical sample-and-hold nature in high-speed, time-interleaved sampled-data systems. Closed-formed expressions will be presented with the verification by numerical computer simulations. Special design techniques and layout issues for reducing both the random process and the systematic mismatches will be presented through a real application of a low phase-skew clock generation circuit that is used for a very high-frequency SC multirate filter with 320 MHz output sampling rate. Measurement results (skew noise tones <-72dBc) will further verify the proposed techniques.

1. INTRODUCTION

The rapid developments of data communications increasingly demand high-speed data conversion and signal processing circuits. Time-interleaved (TI) or parallel-path sampled-data techniques, shown in Fig.1, are one of the efficient ways to maximize the achievable speed in current technology with reduced costs, e.g. time-interleaved ADC [1], N-path [2] or multirate filters. However, the distortion due to the channel mismatches is the bottleneck of such structure for high-performance applications. Also, the errors caused by the timing mismatches become more and more significant for high-speed systems. Such timing-mismatch effects contain the random sampling jitter resulting in an increased noise floor across all frequencies. The magnitude of this increase depends on the slope of the input signal and therefore will increase at 20dB/dec with increasing signal frequency. The output noise power with sampling jitter variance σ_t^2 will be $2\pi^2 A^2 f_{in}^2 \sigma_t^2$ where A and f_{in} are the input signal amplitude and frequency [3-4].

The second effect is the periodic fixed timing skews (or phase-skew) mainly caused by the unmatched but fixed propagation delays among the time-interleaved phases due to systematic-design and process mismatches, as well as switching noise (dI/dt noise). The accurate models for such phase skew effects in the front input sampling stage which result to the nonuniformly sampling have been developed

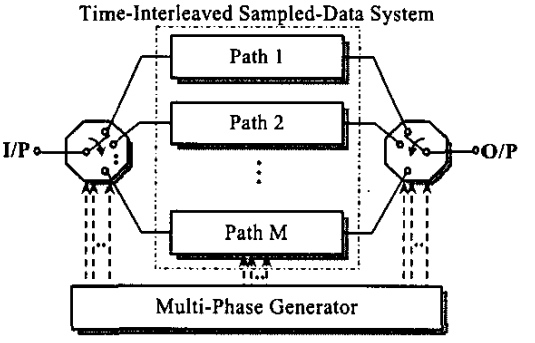

Fig.1 General time-interleaved sampled-data system structure

[5-7]. And the timing-skew effects to the system output signals can be categorized into the following 3 cases:

Case A: *Input nonuniformly sampled, Output uniformly played out (INOU)*

Case B: *Input uniformly sampled, Output nonuniformly played out (IUON)*

Case C: *Input and Output timing-correlatively, Nonuniformly sampled and played out (INCON)*

Typical examples characterized by these 3 cases are TI ADCs, DACs and N-path sampled-data filters respectively, and they were partially investigated in [8] for Case A & C and in [9] for Case B with impulse sampled outputs only. However, except for Case A, the real output signals are sampled-and-held in nature where their output signal spectrum is not simply the shaped version of impulse-sampled spectrum, obtained by multiplying uniform $\sin x/x$ function, thus resulting in different signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR). Hence, this paper will first derive the accurate closed-form expressions for Case B and C. The numerical MATLAB Monte-Carlo simulation results will also be provided to show the SNR and SFDR vs. different input frequencies and skew standard deviations. Then a practical design of a clock generator for a very high-frequency switched-capacitor (SC) multirate filter with 320 MHz output sampling rate, which can be characterized by the Case B with a stringent specification (σ<5 ps), will be presented. Successful measurement results with the worst phase-skew noise tone <-72 dBc will be shown for validating the effectiveness of the proposed design techniques.

2. OUTPUT PHASE-SKEW EFFECTS

Consider the Case B – IUON and suppose the system ideally plays out the uniform input samples at nonuniformly spaced time intervals with holding, i.e.

$$y(t) = \sum_{n=-\infty}^{\infty} x(nT) h_n(t - t_n) \tag{1}$$

where

$$h_n(t) = u(t) - u(t - T - \Delta_{n+1} + \Delta_n) \tag{1a}$$

$$t_n = nT + \Delta_n \tag{1b}$$

and T is the nominal sampling period and Δ_n is a periodic skew timing sequence with period M (path number). Let $n=kM+m$ (m=0,1,...M) and $r_m = \Delta_m / T$, then we have

$$y(t) = \sum_{m=0}^{M-1} \sum_{n=-\infty}^{\infty} x(kMT + mT) h_m(t - kMT - mT - r_m T) \tag{2}$$

Appling the Fourier Transform to $y(t)$, we have

$$Y(\omega) = \sum_{m=0}^{M-1} H_m(\omega) \left(\sum_{k=-\infty}^{\infty} x(kMT + mT) e^{-j\omega kMT} e^{-j\omega mT} e^{-j\omega r_m T} \right) \tag{3}$$

and by substituting the following identities

$$x(kMT + mT) = \frac{1}{2\pi} \int_{-\infty}^{\infty} X(\Omega) e^{-j\Omega(kMT + mT)} d\Omega \tag{3a}$$

$$\sum_{k=-\infty}^{\infty} e^{jk(\Omega - \omega)MT} = \frac{2\pi}{MT} \sum_{m=0}^{M-1} \delta\left(\Omega - \omega + k \frac{2\pi}{MT} \right) \tag{3b}$$

we finally obtain

$$Y(\omega) = \frac{1}{T} \sum_{k=-\infty}^{\infty} A_k(\omega) \cdot X\left(\omega - k \frac{2\pi}{MT} \right) \tag{4}$$

where

$$A_k(\omega) = \frac{1}{M} \sum_{m=0}^{M-1} H_m(\omega) e^{-jkm\frac{2\pi}{M}} e^{-j\omega r_m T} \tag{4a}$$

$$H_m(\omega) = \frac{2\sin(\omega(1 + r_{m+1} - r_m)T/2)}{\omega} e^{-j\omega(1 + r_{m+1} - r_m)T/2} \tag{4b}$$

For the Case C – INCON where the output is described by

$$y(t) = \sum_{n=-\infty}^{\infty} x(t_n) h_n(t - t_n) \tag{5}$$

we can similarly obtain the weight terms to the modulated spectrum sideband of equation (4) as

$$A_k(\omega) = \frac{1}{M} \sum_{m=0}^{M-1} H_m(\omega) e^{-jkr_m\frac{2\pi}{M}} e^{-jkm\frac{2\pi}{M}} \tag{6}$$

The equations (4), (4a) (4b) and (6) fully characterize the output signal spectrum for IUON and INCON cases with nonuniform S/H effects. The results from the MATLAB models built according to the above equations match well with the FFT of the samples with respect to the IUON and INCON sampling processes. Importantly, the equation MATLAB models take much less computation times than that from direct FFT. Fig.2(a-b) and (a'-b') show the mean of SNR and SFDR within Nyquist band vs. (all inversely proportional to) standard deviation (σ) of the skew timing Δ_n and input signal frequencies from 1000-time Monte-Carlo calculations for Case B and C with both S/H output. For comparison, the SNR for 2 cases with impulse-sampled output are also shown in Fig.2c and 2c', where differently, SNR are almost flat over the input signal frequencies.

Besides, Fig.3(a)&(b) are the spectrum of a 58 MHz signal sampled at 320 MHz with the sampling processes Case B and C (M=8, σ=5 ps), respectively, for both impulse and S/H output. Obviously, the modulated imaging sidebands located around f_s/M and its multiples with S/H output are not simply shaped by the uniform sin$x$/x function.

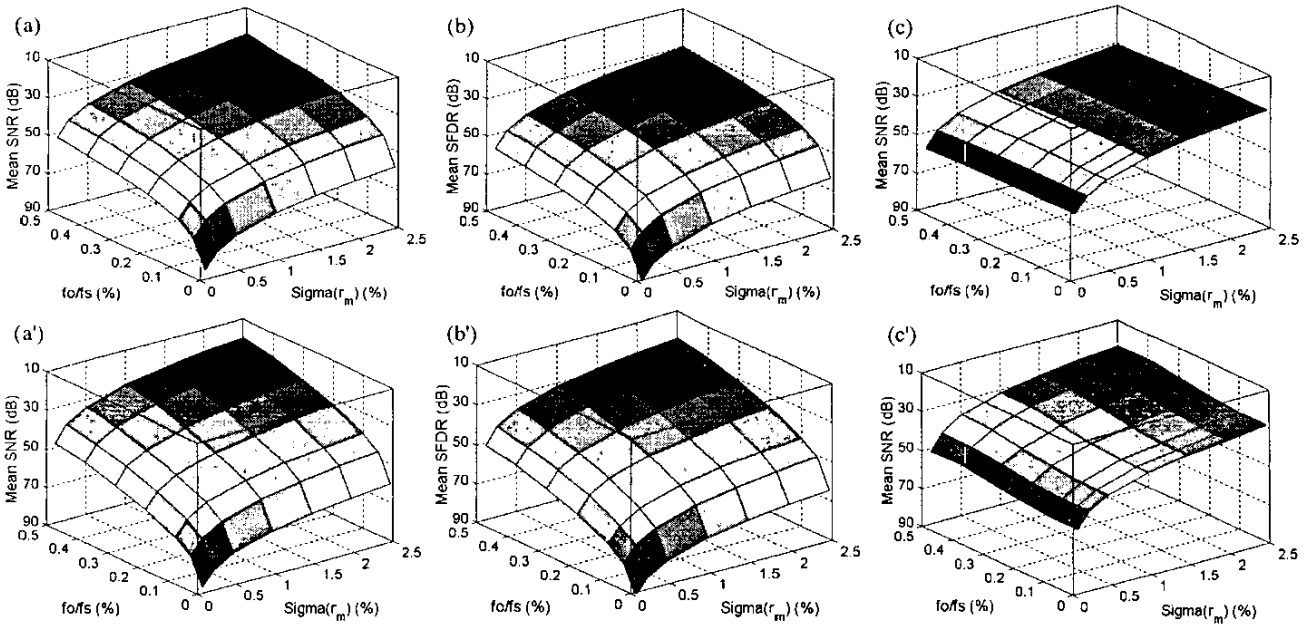

Fig.2 (a) & (a') SNR for S/H output (b) & (b') SFDR for S/H output and (c) & (c') SNR for impulsed output for IUON & INCON vs. input signal frequencies and standard deviation (sigma) of the skew-timing ratio r_m (M=8) by 1000-time Monte-Carlo computations

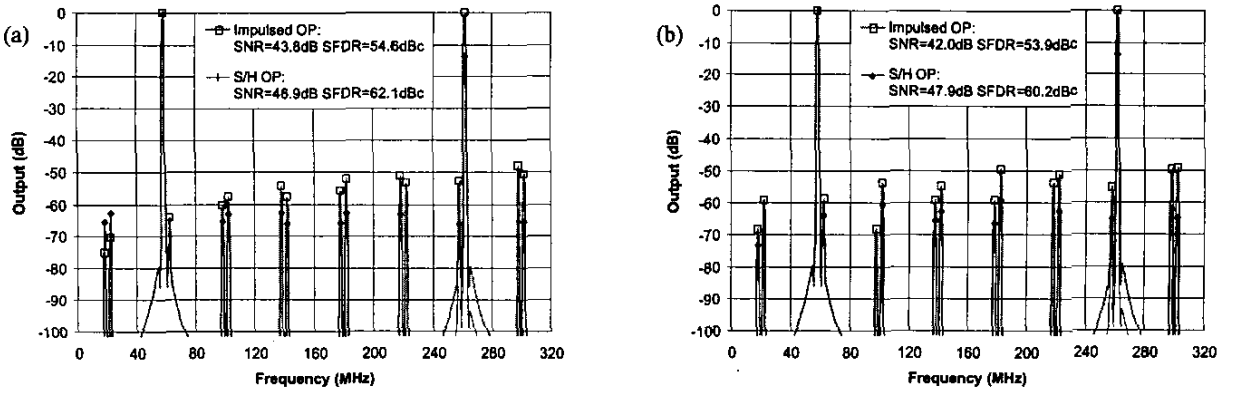

Fig.3 FFT of a 58 MHz signal sampled at 320 MHz for (a) IUON and (b) INCON processes (M=8, σ=5 ps)

3. LOW PHASE-SKEW CLOCK GENERATOR

We present here a multiple phase generator used in a very high-frequency multirate SC bandpass filter that translates 22-24 MHz band to 56-58 MHz with also the sampling rate increase from 80 to 320 MHz for a DDFS system [10]. Due to the S/H nature of input for analog interpolation, the timing jitter effects due to the input sampling of 4 parallel polyphase filter bands are negligible, and thus the timing-skew errors are mainly caused by the last high-speed commutator stage for switching among 4 sub-filter bands at 320 MHz, thus being the case equivalent to IUON. Different from input sampling where the error tones can be shaped by system function, here the resulting modulated sidebands will fold back inside the stopband that cannot be removed by the filter. Thus, from the above investigation, it requires σ<5 ps to ensure the mean SFDR>60 dBc for not degrading the overall system response.

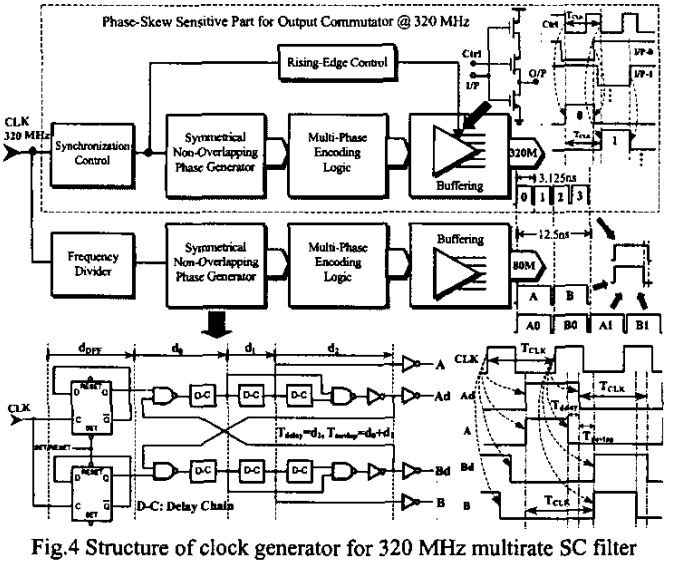

Fig.4 Structure of clock generator for 320 MHz multirate SC filter

The minimization of the phase skews for the clock generator is mainly achieved through the following controls, as shown in the simplified structure of Fig.4:

I. Equal-Propagation-Gate-Delay/Design Systematic Mismatches Control: The accumulated propagation gate delays for all interleaved phases are balanced by careful logic design, e.g. all triggered by same edge of reference: the non-overlapping phase generator shown in Fig.4 with the use of the available standard cells from foundry achieves the rising (also falling) edges of A & B having ideally same pulse width with timing difference of one master clock cycle; dummy gates with buffer trees are used for compensating unbalanced clock distribution. Note that all those designs include the layout parasitic considerations.

II. Output Rising-edge Synchronization/Random Process Mismatches Control: To minimize the random process mismatches imposed from the logic gates. A specific rising-edge synchronizing gate array is designed as shown in Fig.4. It generates 8 phases for the output commutator located just before the last buffers that drive the clock buses. This implies that the mismatch ideally happens only in the last large buffer that can be indeed neglected.

III. dI/dt Supply Noise Control: Individual-on-chip-VDD supply scheme with shared ground and on-chip decoupling for low-speed (filter core) and high-speed (commutator) clock generations are designed to minimize the phase skew imposed by the mismatches in supply voltage variation caused by dI/dt noise. Otherwise, the low-speed clocks, which are the most current-spike consuming part of the whole digital circuit, generate dI/dt noise periodically at maximum 4-time of output sampling period and then destroy the matching of the rising edges of the interleave phases, thus rendering periodically fixed phase skew for output signals. From Monte-Carlo simulations, such skew can be reduced in this way from more than 100ps in worst-case, which will completely degrade the system response, to only about several pico-second level.

IV. Careful Layout: This SC filter is integrated in 0.35 μm double-poly, triple-metal CMOS. All digital cells are customly laid out, due to the stringent tolerance to the phase skew errors, the sensitive high-speed clock part is specially laid out with mirror parallel arrangements for interleaved phases to balance the systematic parasitics and

also with minimized clock bus routing driving the output commutator, as shown in the chip microphotograph of Fig.5. Multi-dimension shielding by lower, same and upper layers with ample contacts to supply so as to reduce the series impedance is used. This avoids not only the digital noise coupling to analog part but also the self-coupling among skew-sensitive clock buses. Some special layout techniques are also used: e.g. special parallel clock-line routing arrangement to minimize the possible disturbance to the rising edges; shielding the clock buses by conductive metal 1 connected to digital VDD to minimize the maximum peak current loop drawn from the bus parasitics at the rising edges of clocks where the originals and their delayed phases are raised at the same time (20% reduction from simulation in supply noise instead of shielding to the common ground); wide-sheet supply lines to minimize the voltage drops across those lines; MOSFET capacitor filled in unused space and under supply lines for enough decoupling capacitance from the supplies to ground.

4. MEASUREMENT RESULTS

The above techniques have been verified by the measurement results. Fig.6 is the measured spectrum of a 58 MHz signal output sampled at 320 MHz by inputting a 22 MHz signal sampled at 80 MHz. The only observed modulation sidebands due to the phase skews (plus also parallel gain mismatches) are at 18 and 62 MHz that are well controlled below –72 dBc, and the sidebands at 22, 102, 138 MHz, which overlap onto the input signal images sampled at 80 MHz, show negligible effect to the system response, as filter achieves desired image rejections at 48, 57 and 51 dB, respectively. Fig.7 is the measured off-chip power supply noise, showing clearly that the unbalance between the low-speed (LS) and the skew-sensitive high-speed (HS) clock parts and the coupling between them is well minimized.

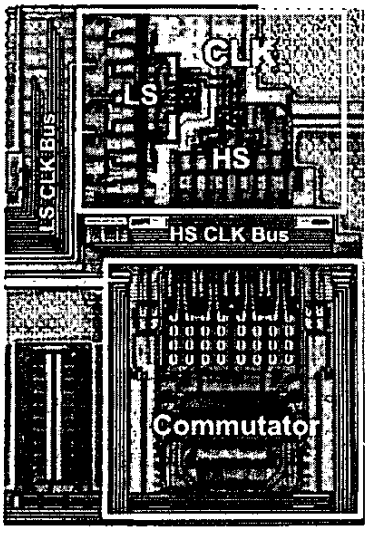

Fig.5 Chip microphotograph for clock generator and output commutator

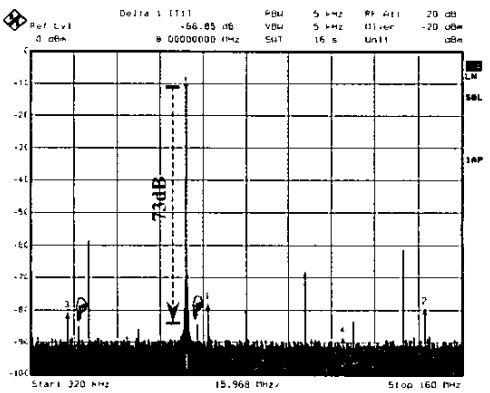

Fig.6 Measured spectrum of a 58 MHz signal output sampled at 320 MHz with a $1V_{p-p}$ 22 MHz input (T&H at 80 MHz)

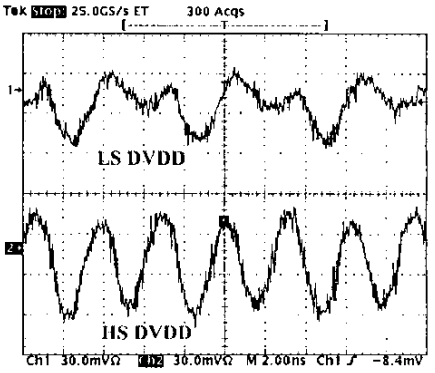

Fig.7 Measured off-chip power supply waveform (DVDD=2.5V)

5. CONCLUSIONS

The clock timing-skew effects including the practical nonuniform sample-and-hold output shaping have been investigated with accurate closed-form expressions verified by numerical simulations. Such expressions can be used to characterize well the DAC systems and time-interleaved sampled-data systems. The design of clock generator for a 320 MHz multirate SC filter has been presented. Both specific circuit design and layout techniques for reducing the mismatches effects have been proposed. Successful measurement results have also been provided for consolidating the effectiveness of the design techniques.

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