

High-Speed Robust Level Converter for Ultra-Low Power 0.6-V LSIs to 3.3-V I/O

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Abstract — A new level converter aimed at ultra-low core voltage and wide range I/O voltage is designed using deep sub-micron process with standard MOS transistor without adding extra mask or process step. Simulation results demonstrate the performance improvement of the proposed level converter which can convert high-speed clock signals from 0.6-V to 3.3-V I/O interface within 0.5ns and maintain 50:53 of duty ratio.

I. INTRODUCTION

The huge market growth of battery-operated portable application increase the demand for low power circuit design, both in digital and mixed signal area. Using extremely low supply voltage for digital logic can improve the power consumption significantly [1]. However, the supply voltage for I/O interface cannot be scaled like this due to the large impedance load and high noise immunity requirement for I/O circuit. For this reason, it is critical to design a robust level converter (LC) which can convert low voltage input signal to I/O signal.

In the paper, we propose a low voltage level converter (LVLC) which is high-speed and robust to input voltage change as well as temperature and process variation. The rest of this paper is organized as follow. Circuit structures of conventional LC will be briefly reviewed in section II and point out how its congenital structures create problems when converting ultra-low input voltage to higher super-threshold output voltage. In Section III, different methods of recent research on level converters is showed and points out the limitations of those methods. The design of the proposed level converter is introduced in Section IV. Section V shows the simulation result and finally conclusion is given in section VI.

II. PRINCIPLE OF LC

Fig. 1 shows the conventional LC which is used for shifting low voltage input to high voltage output. Although the positive feedback of the cross-coupled PMOS transistors improve the switching speed and output swing at typical case, it also cause the LC not function correctly for low input voltage. The level conversion process is shown in Fig. 1, when $MN1$ turns on from '0' to '1', $MN1$ pulls down 'qz' and turns on $MP2$. Since $MP2$ is on and $MN2$ is off, 'q' is charged to '1' and $MP1$ turns off. Notice that $MN1$ and $MP1$ are on

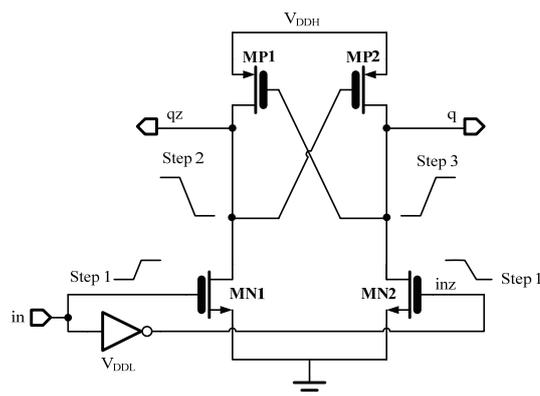


Figure 1. Conventional LC.

simultaneously at the time when $MN1$ turns on. In order to pull down the node 'qz', the pull down (sink) current by $MN1$ should be stronger than the pull up (source) current by $MP1$. Under normal supply of input and by proper sizing $MN1/MN2$, the level converter can function properly. When the input voltage decrease further near threshold voltage of $MN1$, the sink current from $MN1$ will further decrease and soon $MN1$ cannot obtain appropriate pull down strength to overcome the current from $MP1$ [2]. The node 'qz' therefore cannot be pulled down and the positive feedback cannot be ignited immediately. The LC either suffers from large delay or cannot function correctly as a result. This problem is critical when it is used to convert clock signal in high speed analog and mixed signal design.

III. EXISTING LVLC

Recent research is focused to overcome this problem. In [6], thick native devices which have a very low threshold voltage (V_t) are used. As shown in Fig.2, thin oxide devices $MN1/MN2$ are used and the thick oxide native devices $MN5/MN6$ aims to prevent thin oxide devices from the high voltage supply. Using thin oxide devices, which has lower V_t , can strengthen the sink current. However, the introduction of native devices increase the cost and complexity during mask production which is not preferable for modern industrial design work. Moreover, the solution proposed in [2] use

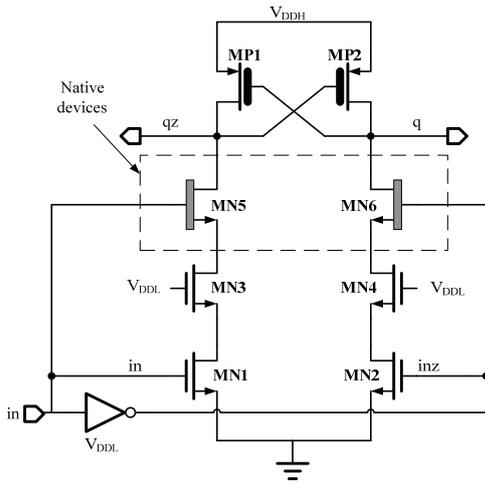


Figure 2. Use of zero V_t native devices for LC in [6].

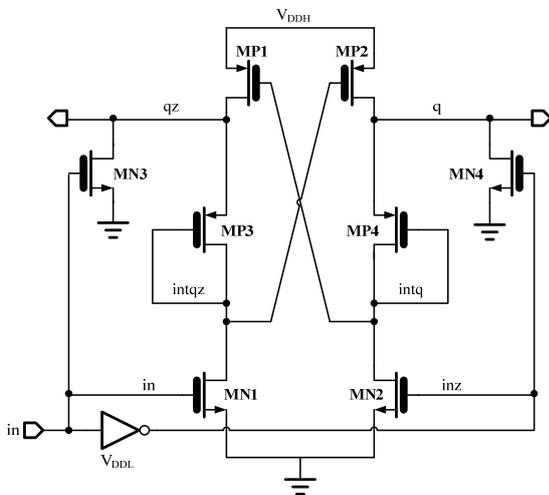


Figure 3. Sub-threshold LC in [8].

voltage doublers to “pump” up input voltage to increase the pull down strength from the pull down transistors. However, the input voltage for the voltage doublers should be high enough to ensure that it can work properly, and it is not executable for ultra-low power application. Moreover, the new added voltage doublers instead will increase area and power consumption which is also not preferable.

Although we have assumed that the MOS device turns off abruptly as the gate voltage of the transistor approaching V_t , a “weak” current flows still exists from drain to source even when $V_{GS} < V_t$. The current will be exponential dependence on V_{GS} [3,4,7]. This current should enough to act as sink current if the source current is well suppressed. In [5], a reduced swing inverter is introduced to limit the voltage swing at the gate of the two pull up transistors to minimize the source current. As the sink current is relative stronger compare with the source current, the cross-couple feedback can then be activated. But it has been shown in [8] that the addition of inverter will limit the acceptable input logic voltage and the pull up ability of the two pull up transistors.

Fig. 3 shows the sub-threshold LC proposed in [8]. By employing 2 PMOS diodes as shown, the source current can be well suppressed. The diode connected $MP3$ & $MP4$ help to minimize the source current from $MP1$ & $MP2$. When the LC is at steady state, the diode voltage drop $|V_{PD}|$ is very small. When input of $MN1$ change from ‘0’ to ‘1’, the diode voltage drop of $MP3$ will not change so quickly and it maintains at its initial value of $|V_{PD}|$, which limits the pull up strength of the left branch. At this time, $MN1$ weakly turn on and this “weak” sink current will pull down the voltage at node ‘intqz’ which is then turn on $MP2$ in the right branch and activates the cross couple positive feedback [8].

Although the introduction of diode can solve weak pull down problem from $MN1/MN2$, this diode limit the output swing of LC due to the voltage drop from the diode. When the LC is pull down in either branch, the output cannot pull to ground as it is one $|V_{PD}|$ higher than ground. For this reason, in [8], it suggested two NMOS transistors $MN3$ & $MN4$, which is control by the input of pull down transistors, to directly discharge the output to ground. However, the current from $MN3/MN4$ is not strong enough to pull down the output when core voltage is slow. In our simulation, however, this technique has been proven failed to convert high speed clock signal as the LC cannot ground completely and immediately within a short period of time.

IV. PROPOSED LVLC

In mixed signal design, LC can be used to convert clock signal to I/O supported voltage for the use of the blocks with high noise immunity. The limitations of LC in [8] cause critical problem when using in such application. In order to make the LC work correctly at high-speed for ultra-low core voltage, a novel LVLC is proposed as shown in Fig. 4. Here we introduced two pairs of pull down switches $MN3/MN4$ & $MN5/MN6$. Both pair of switches work in parallel and have different purposes. The interactions of them speed up overall performance of the LC.

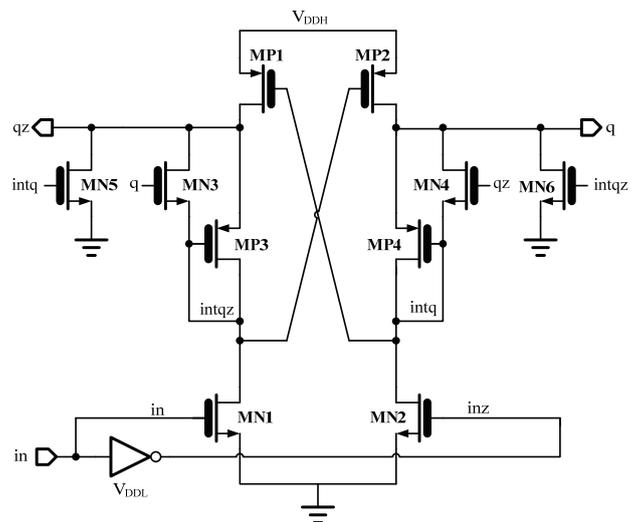


Figure 4. Proposed LVLC.

The pair of switches strengthen the pull down current and speeds up the pull down operation of the LC. In Fig.4, the NMOS transistors $MN3/MN4$ directly shorted output to node 'intqz' & 'intq'. They are controlled by the output in order to provide a stronger current. When input of $MN1$ change from '0' to '1', the cross couple positive feedback is activated, so $MP2$ is on and $MP1$ is off. Output node 'q' being shorted to ground will start to rise to V_{DDH} as node 'qz' drop to a certain level. Then, $MN3$ which is controlled by node 'q' strongly turn on and the node 'qz' can completely shorted to ground through $MN1$. However, as the source of $MN3/MN4$ are connected to node 'intqz' & 'intq', the rate of voltage drop at these node are determined by the sink current by $MN1/MN2$ which usually takes time and affects the pull down speed at output.

With the help of two NMOS switches $MN5/MN6$ which directly short node 'q' and 'qz' to ground, the previous problem can be solved. Notice that the switching operation shouldn't be controlled by output node 'q' and 'qz' which will cause voltage translation problem as a result. Therefore, internal node 'intq' & 'intqz' are then used as the gate control of $MN5/MN6$. However, this internal node voltage level is strongly dependent on the supply voltage V_{DDH} . Therefore, when converting low supply I/O, although $MN5/MN6$ is off, $MN3/MN4$ can operate alone and should be enough for the pull down. The reason is that at low supply V_{DDH} , the rate of voltage drop at node 'intq' & 'intqz' is larger which favors the pull down operation of $MN3/MN4$.

For this reason, the sizing ratio on these two pair of switches depends on the supply of I/O. When converting to high supply I/O, the sizing ratio on $MN5/MN6$ should be large and vice versa. Usually we use the same size of switches to get balance rise/fall time. Moreover, in our design, $MN1/MN2$ should be powerful enough for the sink current. This can be done by sizing $MN1/MN2$ or the two diode connected $MP3/MP4$. The size of diode depends how the source current is suppressed.

V. SIMULATION RESULTS

The proposed level converter is designed in deep sub-micron CMOS technology. The conventional LC and the LC in [8] are also implemented with same transistors size for fair comparison. A 50fF capacitance is attached at the output as a realization of logic gate loading. We use HSPICE simulation to check the performance and power consumption.

The first experiment is to show the improvement of the propose LVLC. The proposed LVLC and LC in [8] are compared. A 0.6-V input clock signal at 10MHz is fed into both LCs. Fig. 5 shows the result. From the result, we can see that the LC in [8] fails to work when converting high-speed clock signal. Next, we have to estimate how the proposed LVLC response to the conversion of different core and I/O voltage. A 0.6-V input clock signal at 100MHz is fed into the LVLC and convert to I/O voltage at 1.8V, 2.5V and 3.3V. The process is repeated for different core voltage. Simulation is performed in typical case and the result is shown in Fig. 6.

To further verify the improvement of level converter, the proposed LVLC and LC in [8] are compared. Fig. 7 shows the

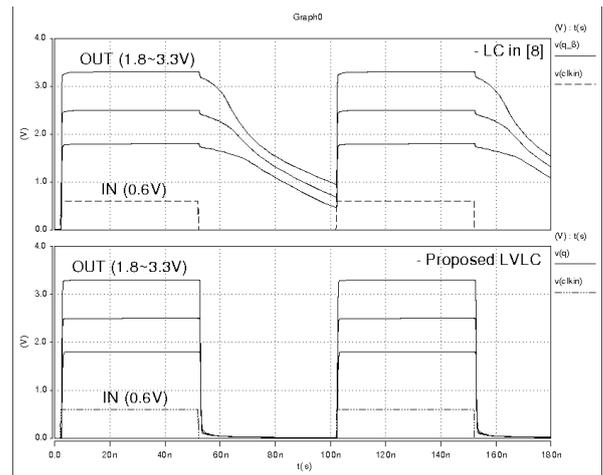


Figure 5. Simulation result with 10MHz signal (Top: LC in [8]; Bottom: Proposed LVLC).

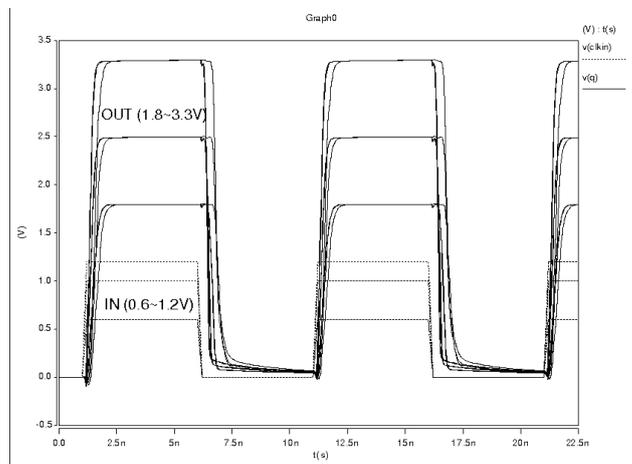


Figure 6. Simulation waveform of LVLC @100MHz

shmoo plots for them. In this simulation, we fed with 10MHz clock signal and V_{DDL} and V_{DDH} is varied from 1.2V to 0.4V and 3.3V to 1.8V respectively. The shmoo plot mark a 'pass' as the LC can completely convert a rail to rail clock signal, so this plot can shown in what condition the LC work. As shown in the figure, our proposed LVLC is more robust to voltage variation as compared with the LC in [8].

In the design of high noise immunity blocks, LC is used to convert clock signal to I/O supported voltage. For this reason, it is important that the LC response quickly to clock signal without delay and can maintain its duty ratio. The last simulation here is to check and compare how the output delay in time and duty cycles changes with the input voltage. Clock signal at 10MHz is scaling down from 1.2V to 0.5V and is fed into three different types of LCs separately. The duty cycles are calculated from the output and the result is plotted in Fig.8 (a). From the plot we can see the conventional LC fails to work when input is lower than 0.6V while the LC in [8] gets a very poor duty ratio. Our proposed LC can maintain 57% of duty cycles even the input voltage is at 0.5V. Fig.8 (b) plots

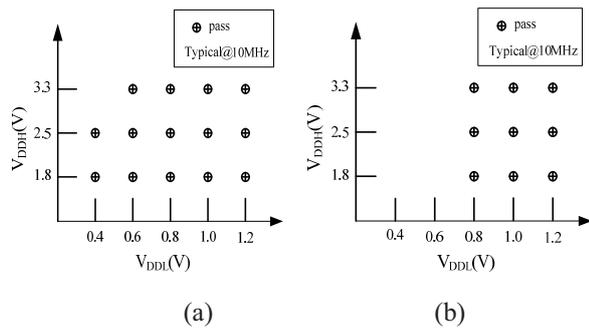
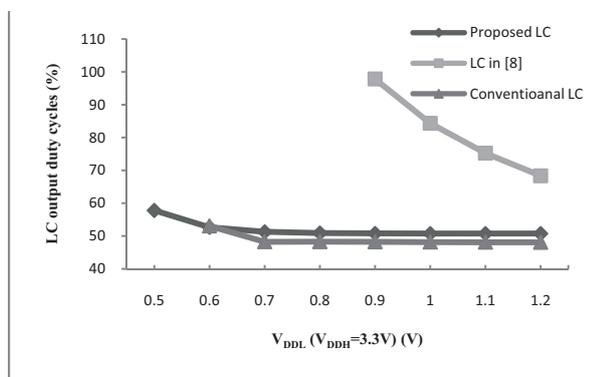
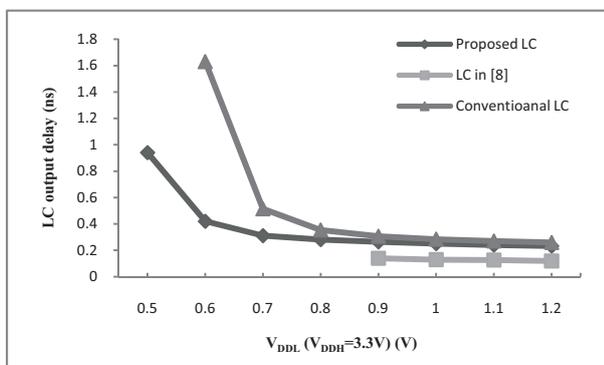


Figure 7. Shmoo plots of (a)Proposed LVLC (b)LC in [8].

also the output delay in time for these three different types of LCs. From the plot, we can see that although the conventional LC works at voltage as low as 0.6V, it is still a disaster for high speed application for such a huge output delay. Finally, a summary of the simulation performances is listed in Table 1.



(a)



(b)

Figure 8. LC (a)duty cycles (b)output delays vs V_{DDL} .

TABLE I. SUMMARY OF THE LVLC PERFORMANCE

$V_{DDL}(V)$	$V_{DDH}(V)$	Rise Time (ps)	Fall Time (ps)	Power Consumption (μW)	Duty Cycle (%)
0.6	1.8	493	486	219.35	52.97
	2.5	412	492	546.69	52.67
	3.3	433	499	1116.7	52.66
1.0	1.8	471	284	243.78	51.66
	2.5	356	220	601.56	51.01
	3.3	303	194	1203.6	50.76
1.2	1.8	470	279	254.55	51.64
	2.5	356	219	614.36	51.00
	3.3	303	193	1219.1	50.73

VI. CONCLUSION

In this paper, we proposed a new LVLC. With the introduction of two pull down switches working in parallel, the proposed circuit can improve slow fall time problem which can robustly convert 0.6~1.2V input voltage to 1.8~3.3V I/O interface within 0.5ns. Fabrication complexity is reduced as standard MOS transistor is used. With stable duty ratio and wide output range make this LC suitable for high-speed ultra-low core voltage LSIs.

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