Model, Characterization and Solutions of Unstable Reference Voltage for Very-High-Speed Pipelined A/D Converters

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Abstract - **The principle of pipelined analog-to-digital converter (ADC) is to subtract sequentially different reference voltages along the cascaded sub-ADCs. Such an operation unpleasantly forces the loading of the reference voltage generator features input-dependent fluctuation, which consequently induces irreparable distortion to the signal being converted. This paper presents an in-depth investigation on the causes and effects of unstable reference voltage. Both dynamic and static error sources are characterized and modeled. Effective off-chip and on-chip compensation methods for improving the reference voltage stability are also proposed.**

Index Terms - **Analog-to-Digital Converter (ADC), Pipeline, Reference Voltage, Model, Noise**

I. Introduction

Very-high-speed and medium-resolution pipelined analog-to-digital converter (ADC) finds applications in modern communication systems such as high-IF-sampling cellular receiver, digital-IF broadcast TV base-station receiver, and electronic equipments like RGB flat panel displayer [1]-[3]. Without the need of any parallelism, such kind of Nyquist ADC to date can achieve not less than 220-MHz sampling rate with also 10-bit resolution in deep-submicron standard CMOS [4]. To achieve such stringent speed-and-resolution requirement and determine the circuit-level specifications both accurately and rapidly, a system-level model that provides enough degree of abstraction of the system behaviors is undoubtedly essential. In the literatures, numerous model [5]-[6] and calibrations [7]-[8] of circuit non-idealities have been proposed. Their focuses are mainly put on the effects of op-amp finite gain and gain-bandwidth product (GBW), slew-rate limitation, components mismatch and clock-jitter noise, etc. However, to the best of our knowledge, it is still lack of comprehensive investigation on the causes and effects of unsteady reference voltage generator, which becomes one of the dominant noise sources of pipelined ADC that cannot be underestimated in very-high-speed operation. This paper concentrates on such matter presenting thorough analysis as well as effective model techniques and solutions. Although the analysis is carried in general single-channel 1.5-bit resolution per stage pipelined ADC, the model techniques and presented results are applicable to other enhanced pipelined ADC architectures such as time-interleaved or double-sampled since all channels typically share the same reference generator.

After this introduction, Section II presents the operating mechanism of pipelined ADC that forces the reference voltage, V_{ref}, fluctuates according to the input variation, and simultaneously quantifies the significance of such error with respect to the key performance metrics, e.g., effective number of bits (ENOB) and spurious-free dynamic range (SFDR). In addition to such dynamic error, in Section III, the noteworthy static errors due to negative and positive DC offsets (their effects are different) and random-noise modulation are studied and modeled. In Section IV, the issues related to stabilization techniques through the use of large off-chip capacitor are addressed, which focuses on the problem of package-inductance-induced oscillation and some improved modifications are suggested. Accordingly, two novel on-chip compensation techniques are presented. Their advantageous features and necessitated overheads are also discussed. Finally, certain conclusions and design suggestions are summarized in Section V.

II. Dynamic error: Input-dependent fluctuation on reference voltage

A. *Source of dynamic error*

The most significant input-dependent error voltage is due to the dynamic loading effect, which can be described by Fig. 1. At phase 1 (phase 2), the sampling capacitor C_s in the even (odd) stages requires either $-V_{ref}$, 0 or V_{ref} voltage to accomplish the stage digitization as well as signal passing. Thus, in every half of sampling period, the loading point of reference voltage buffer, $V_{ref}(nT_s/2)$, loses its original precision with different amounts, which highly depends on the total loading (i.e., the number of capacitor C_s) connected to the buffer at such instant. Undesirably, connecting either $-V_{ref}$, 0 or $+V_{ref}$ to the stage is determined by the digital output codes m {-1, 0, +1} generated from their stage sub-ADCs (flash-type ADC), which determine the stage analog input is either $< -V_{ref}/4$, $[-V_{ref}/4, V_{ref}/4)$, or $\geq V_{ref}/4$. As a result, this operation undesirably links the total capacitance loaded on the buffer to the signal variation. Thus, such error is classified as a dynamic error. To quantify such dynamic error to performance degradation, a system-level model that includes all the generic functionalities of pipelined ADC is proposed in the following.

B. *Model of dynamic error*

Denoting the digital output code of the k^{th} stage sub-ADC in each half of sampling period as $m_k(nT_s/2)$, which equals either -1, 0 or +1. The total capacitor loaded on the buffer is then given by

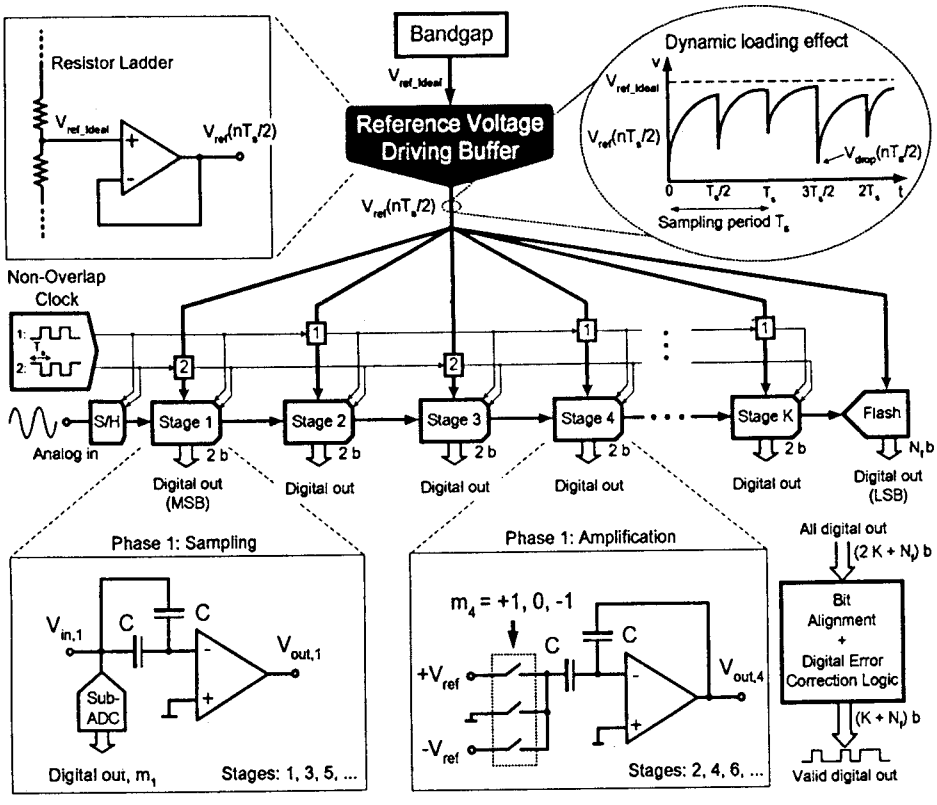

Fig. 1 A generic switched-capacitor 1.5-bit/stage pipelined ADC. The number of stage K is assumed to be an even positive integer.

$$C_{eq}(nT_s/2)=\begin{cases}\sum_{k=1}^{\lfloor (N-N_f)/2 \rfloor}\left(C_{s,2k-1}\cdot\left|m_{2k-1}(nT_s/2)\right|\right) & \text{for } n=1,3,5\ldots\\ \sum_{k=1}^{\lfloor (N-N_f)/2 \rfloor}\left(C_{s,2k}\cdot\left|m_{2k}(nT_s/2)\right|\right) & \text{for } n=2,4,6..\end{cases} \quad (1)$$

where $C_{s,k}$ is the sampling capacitor at stage k. N and N_f are the resolution of the entire ADC and the last stage sub-ADC, respectively.

As depicted in Fig. 1, the transient voltage drop, $V_{drop}(nT_s/2)$, will be continuously compensated by the buffer until the end of the clock period such that the final value will be injected to all stages. The precision of V_{ref} that can be recovered obviously depends on the size of the capacitive loading (i.e., total number of C_s) and the speed of the buffer's op-amp (i.e., slew rate (SR) and GBW). To determine these parameters, maximum value of the transient voltage drop, $V_{drop,\,max}$, must be found.

In the extremely case, each sampling capacitor loaded on the V_{ref} buffer stored $V_{ref}/4$ that equals to the threshold of the sub-ADC. If all C_s are equal in size, the $V_{drop,\,max}$, of an N-bit ADC is given by,

$$V_{drop,\,max}=\frac{V_{ref}}{4}+\frac{3}{4}V_{ref}\left(1+\frac{C_s}{C_p}\cdot\left\lceil\frac{N-N_f}{2}\right\rceil\right)^{-1} \quad (2)$$

Assuming that the buffer's op-amp is a non-linear single-pole system, there are two ways to find the minimum SR, SR_{min}, and GBW. First, when the SR is sufficient, only the GBW takes effect to settles the V_{ref},

$$V_{ref}=\left(V_{ref,ideal}-V_{drop}\right)+V_{drop}\cdot\left(1-e^{-t/\tau}\right) \quad (3)$$

This leads to the SR_{min} value that results in non-slew settling equals to the maximum gradient of the linear settling output curve as given by,

$$SR_{min}=\frac{\left|V_{drop}\right|}{\tau} \quad (4)$$

where $\tau=\dfrac{1}{2\pi\cdot\beta\cdot GBW}$

is the settling time constant and β is the feedback factor of the buffer. However, when the SR is smaller than the value given by (4), op-amp enters non-linear operation (i.e., slewing with linear slope SR) until the remaining voltage is smaller than $SR_{min}\cdot\tau$, and then it starts to settle exponentially. The reference voltage with non-linear settling yields,

$$V_{ref}=V_{ref,ideal}-\left[V_{drop}-SR_{min}\cdot t_0\cdot sign\left(V_{drop}\right)\right]\cdot e^{\frac{-(t-t_0)}{\tau}} \quad (5)$$

where $t_0=\dfrac{\left|V_{drop}\right|}{SR_{min}}-\tau$.

Founded by (1)-(5), the ENOB of the entire converter, in terms of the precision of driving buffer and the entire

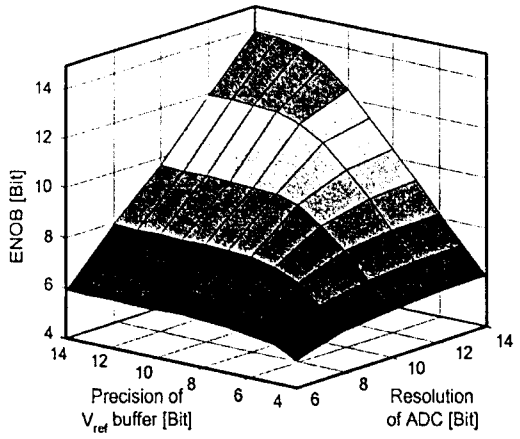

Fig. 2 V_{ref} buffer precisions versus ENOB for different ADC resolutions.

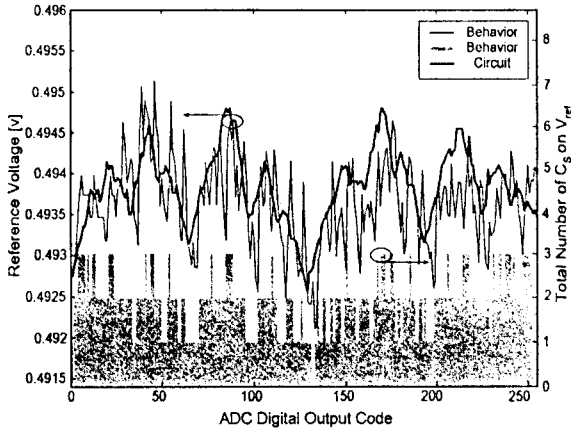

Fig. 3 V_{ref} buffer precisions versus ENOB for different ADC resolutions.

ADC resolution, is plotted in Fig. 2. It shows that the appropriate precision of the voltage reference is 1 bit less than the required of the ADC, precision higher than that is generally exhausted. Such model is verified by comparing the behavioral simulations obtained in Matlab™ with the one obtained through circuit simulation in Cadence™. A full-scale ramp input signal resulted V_{ref} variation is plotted in Fig. 3, where the total number of loading capacitor (maximum 3 stages for K=6) is also shown there. The simulation conditions include 200-MHz sampling rate, 8-bit resolution and 0.5-V reference voltage. As it can be observed from Fig. 3 that the accuracy of the model is average high, the fluctuating tendency is well predicted and follows the variation of the total number of loading. Such tendency importantly helps to quantify the magnitude of the distortion components. Solutions for this error are presented in Section IV.

III. Static errors: DC offset and random-noise modulation on reference voltage

A. DC offset

V_{ref} is one of the parameter for setting both input and output full-scale range, and thus any offset voltage will undoubtedly limits the full-scale (FS) signal that can pass through the stages. Offset voltage in the reference, which regularly exists due to unavoidable components mismatch, is random in polarity (either positive or negative). Such mismatch may come from the bandgap, resistor ladder and/or output driving buffer. This kind of error is mostly static and their total effects can be observed on the overall A/D conversion curve as shown in Fig. 4(a) together with the time-domain illustrations (10-bit resolution is assumed). The negative and positive DC offset induced errors are quite different in consequences. On one hand that the negative offset shorten the conversion range, and leads to saturation once the input signal amplitude is larger than the reference value. Such rail-to-rail clipping is undoubtedly a hard distortion that results significant lost in the ENOB and SFDR [Fig. 4(b)]. On the other hand, positive offset only lengthen the conversion range and consequently degrades the signal-to-noise ratio (SNR) more [Fig. 4(c)]. To deal with such error by post-fabrication calibration or trimming is possible (e.g., by using switched-resistor bank in the resistor ladder [Fig. 1]).

B. Random-noise modulation

Random noise is indubitably the underlying limitation of most kinds of ADC to achieve high resolution. Given that reference voltage is a DC signal, flicker noise generated from the buffer's op-amp is a dominated noise source. The resulting effect can be considered as a random modulation as it is mostly signal independent. The model approach for such noise is as follows:

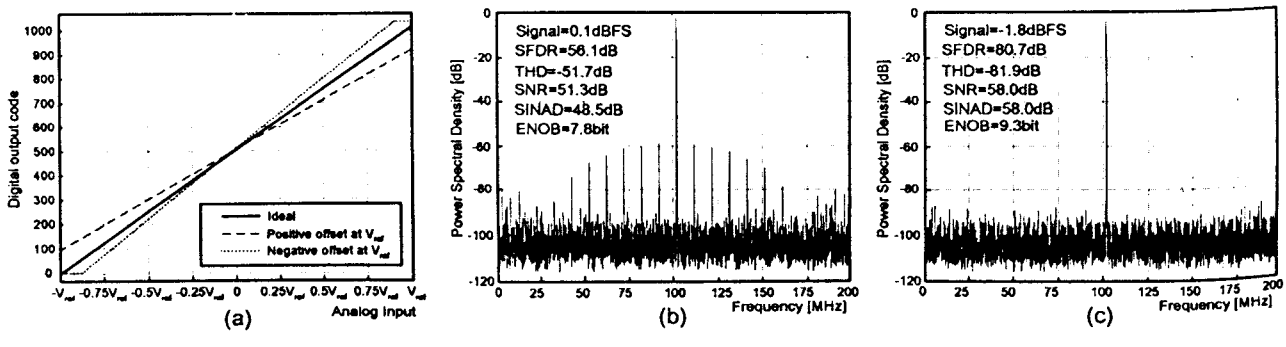

Fig. 4 (a) The resulted errors of positive and negative V_{ref} offset in A/D conversion curve. Influence to the entire ADC performance due to (b) negative offset and (c) positive offset.

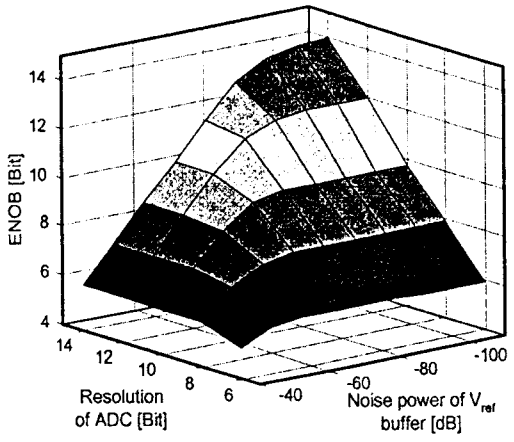

Fig. 5 Noise power on V_{ref} buffer versus ENOB in terms of ADC resolutions.

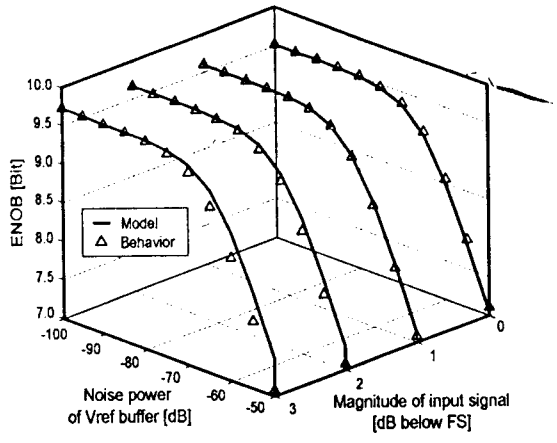

Fig. 6 Noise power on V_{ref} buffer versus ENOB in terms of input magnitude (10-bit ADC).

Noise exists in the reference is directly added to the sampled-values in the capacitors C_s when the output of reference buffer (either $-V_{ref}$ or $+V_{ref}$) is required during the amplification phases. In order to describe the nature of this effect the relationship between the sampled-input, analog output and non-ideal V_{ref} can be found first. Denoting $V_{in,k}$ as the k^{th} stage analog input, its corresponding analog output from the multiplying digital-to-analog converter (MDAC) is given by,

$$V_{out,k} = (2^{N_{eff}}) \cdot V_{in,k} - \left[\sum_{d=1}^{2^{N_{eff}}-1} (m_k(d)) \right] \cdot V_{ref} \tag{6}$$

where $m_k(d)$ is the digital output code from k^{th} stage sub-ADC. The sample-dependent variables on the input $V_{in,k}$, output $V_{out,k}$ and V_{ref} are omitted for simplicity. With input referred noises and random noise at the reference, the corresponding output is denoted as $V_{out\_in,k}$ and $V_{out\_ref,k}$. (6) can be re-expressed as follows,

$$V_{out\_in,k} = V_{out,k} + \left(2^{N_{eff}} \right) \cdot \sigma_{input} \tag{7a}$$

$$V_{out\_ref,k} = V_{out,k} + \left[\sum_{d=1}^{2^{N_{eff}}-1} (m_k(d)) \right] \cdot \sigma_{ref} \tag{7b}$$

where σ_{input} and σ_{ref} are the standard deviations of random noise at the input and at the reference, respectively.

From (7a)-(7b), it is worth to mention that noise in V_{ref} affects the conversion range differently with the input referred noise since the sampling capacitor C_s has chance to connect to common mode voltage (i.e., $m_k(d) = 0$) which is much more stable than the reference voltage as it is predominately loaded by certain amount of un-switched capacitors. Thus, the V_{ref} noise contribution is sometimes less than the other input-referred ones. However, the digital output code $m_k(d)$ is input dependent, worst-case consideration makes the conversion range cannot be optimized. However, the worst case must be considered in the model. Therefore, noise in V_{ref} is assumed to be purely input referred as given by,

$$\sigma_{in\_ref,k} = (\sigma_{ref,k}) \cdot \frac{\sum_{d=1}^{2^{N_{eff}}-1} \left(1 - \frac{d}{2^{N_{eff}+1}} \right)}{2^{N_{eff}}} \tag{8}$$

where a full-scale ramp input is assumed.

For instance, the impact of random noise exists in a 0.5-V reference voltage to the entire 1.5-bit/stage pipelined ADC performance, is plotted in Fig. 5. Focus on 10-bit resolution, the degrading of ENOB as a function of reference voltage noise is compared in Fig. 6 based on both (6)-(8) and behavioral simulations. The result not only shows good agreement to each other, but also proves the impact of noise exists in V_{ref} is related to the input signal. Thus, an optimized amplitude value for the input signal must exist such that the approximation is the finest, which is found to be 1 dB below full scale. It is well-known that V_{ref} limits the minimum voltage of common mode, noise exists in V_{ref} therefore also reduces the voltage headroom for low-voltage design. Furthermore, similar to general DC buffer's op-amp design, large transistors device size is highly desired to minimize the flicker noise once the speed degradation is still uncritical.

IV. Reference voltage stabilization techniques

A. Off-chip stabilization

The simplest way to reduce the fluctuations on the V_{ref} due to dynamic loading and random-noise modulation is by adding a relatively large external capacitor that acts as a dominant load for the reference buffer. When such capacitor is fully charged after transient, switching activity among the rest capacitors does neglectable effects. Another advantage is such capacitor can be used for compensation when multistage op-amp is employed in inverting op-amp configuration buffer, then the output impedance of the buffer would be extremely low at all frequencies and consumes little power [9].

The effectiveness of this method is studied by the proposed macromodel depicted in Fig. 7, which models the capacitive load of the driving buffer from odd and even stages as two sets of capacitor pair. All the capacitors are pre-charged with distinct voltage levels to

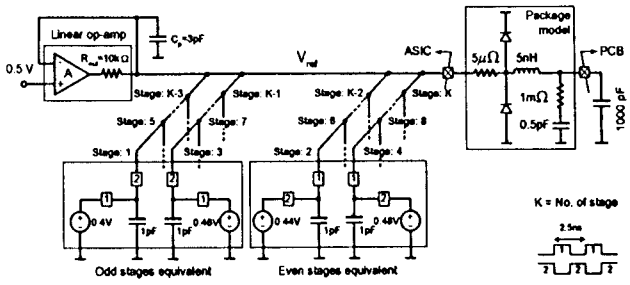

Fig. 7 Proposed macromodel of V_{ref} generator with external capacitor.

emulate the unknown stored charge from the previous stage. For the buffer, the op-amp is a single-pole linear system with GBW equal to $A_o\omega_o$ and close-loop output resistance equals to the open-loop output resistance R_{out} divided by the DC gain A_o. The two-phase operation is driven by two non-overlap clock phases, namely 1 and 2.

Firstly, consider an example based on such model without the package and external capacitor. At phase 1, the odd stages equivalent capacitors are charged with 0.4 V and 0.46 V while the even stages ones are connected to V_{ref}. Similar operation runs at phase 2 with different pre-charged voltages. The sampling frequency is assumed to be 400 MHz. The resulted V_{ref} is plotted in Fig. 8(a). Such value is designed as 0.5 V originally. The static voltage drop from 0.5 V to approximate 0.48 V is due to the switching capacitors, which behave as a resistor that loaded the V_{ref} at such high sampling rate (the resulting degradation of this effect is similar to the negative offset problem as described in Section-III-A). When the clocks are switching, at the beginning of every phase either 1 or 2, the pre-charge voltages in the odd or even stage equivalents will be averaged. Then, the buffer provides current to compensate such charge loss. Undoubtedly, the precision will be highly degraded once the compensating speed is insufficient. This fact governs the minimum power required for the op-amp and the size of the compensation capacitor that needed.

For instance, to overcome such effect by using a linear single-pole op-amp (60-dB DC gain and 1-Grad/s GBW) together with a 1000-pF capacitor connected to the buffer's output, a highly stabilized V_{ref} is obtained in Fig. 8(b). Such large capacitor regrettably occupies huge chip area if it is fully implemented on-chip. Rather, in off-chip approach, the mutual inductance in the package bondwires will resonate with such capacitor as illustrated in Fig. 8(c) (5 nH is taken as the bondwire effective inductance). For those large values of capacitance and inductance, the resonant frequency is easy to be inside Nyquist and therefore highly degrades the spectral purity. One solution for that is to reduce the bondwire inductance through parallel use of bondwires, which however raises the package cost and may not be always possible. Another solution is by adding a resistor R (e.g., 100 Ω) in series with such capacitor and bondwire to damp such oscillation [Fig. 8(d)]. This way is effective to damp the resonance exponentially and shorten the settling time, but not the transient voltage drop since the bondwire provides a high impedance at the transient period. In other words, it isolates the reference buffer to the external capacitor temporarily. This effect is not important once the transient voltage drop is not very

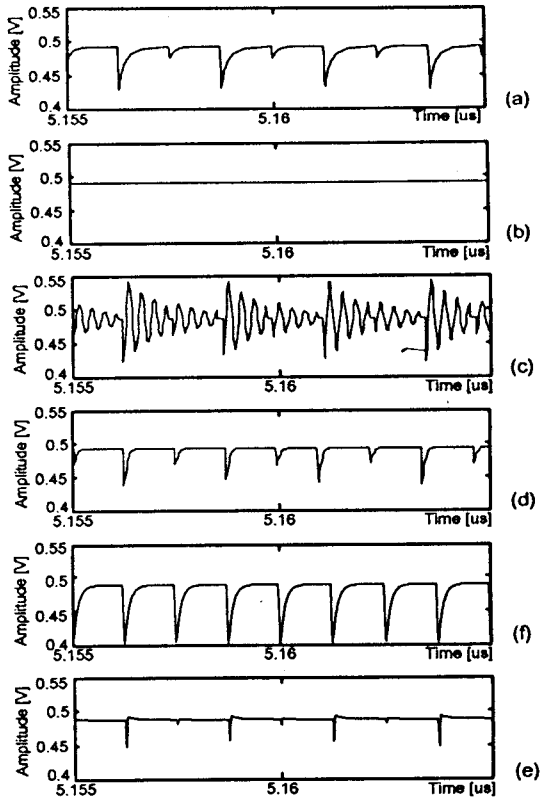

Fig. 8 Simulated reference voltages. (a) No stabilization. (b) With 1000-pF stabilization capacitor on-chip. (c) With 1000-pF stabilization capacitor off-chip. (d) Case (c) with another 100-Ω resistor added in series. (e) On-chip stabilization method 1 and (f) method 2.

deep, since only the finally settled value is important [10].

B. On-chip stabilizations

Two novel purely on-chip stabilization methods are proposed. Both solutions are conducted by adding a compensational branch to the classical MDAC.

Method 1: Constant-charging capacitor V_{ref} compensation

The second method is shown in Fig. 9. This circuit is known for many years for low-voltage application, however, it is not employ for eliminate the unsteady reference voltage. The reference voltage is now injected by using an additional capacitor C_C which charged to V_{ref} during sampling phase. At the next phase, C_C either discharge for reference injection or self-reset. Consequently, reference voltage will not be affected by the input signal; it just exhibits a constant voltage drop at each sampling instance as shown in Fig. 8(f). The size of the C_C should be identical to C_s and C_f. The main overhead is the feedback factor which degrades from 1/2 to 1/3.

Method 2: Correlated-double sampled V_{ref} compensation

The modified MDAC is showed in Fig. 10 single-endly. In order to eliminate the input dependence, at the

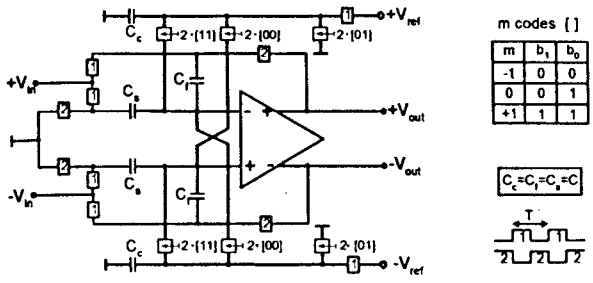

Fig. 9 Modified MDAC of Method 1 with V_{ref} compensational branch.

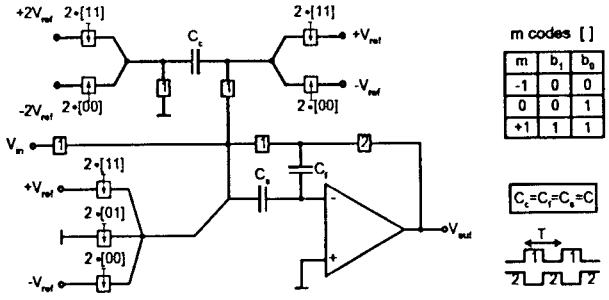

Fig. 10 Modified MDAC of Method 2 with V_{ref} compensational branch.

sampling phase (phase 1), the input signal not only sampled by C_s and C_f, but also sampled by C_c such that it can be used for compensation in phase 2. Considering there are three cases for different values of m: when m=+1 (-1), C_c is connected to V_{ref} ($-V_{ref}$) and $+2V_{ref}$ ($-2V_{ref}$), thus results in no transient voltage drop, or keeps the voltage drop equals $+V_{ref}$ ($-V_{ref}$). For m=0, C_c connects to common mode so as to perform only signal amplification and self-reset. The DC voltage $\pm 2V_{ref}$ can be simply generated by resistor ladder since their accuracy is not important. Any offset caused by the resistor ladder results in constant voltage drop like DC offset (Section-III-A). The simulated performance of this method is shown in Fig. 8(e). It is worth to mention that the voltage drop in Fig. 8(e) is due to current draw by the $\pm 2V_{ref}$ resistor ladder which is slightly related to the input. However, such resistor can be designed to be very small through parallelism, thus the recovery speed is extremely fast. The drawback of this solution is an increase in the loading capacitance on the MDACs from $2C$ to $3C$ during the sampling phase.

V. Conclusions

An exhaustive analysis on the causes and effects of unstable reference voltage to the performance degradation of very-high-speed pipelined ADC was presented.

The pipelining operation creates an input-dependent loading effect on the reference generator. Featuring such input-dependent dynamical characteristic not only forcefully pollutes the output spectrum of the ADC, but also prohibits calibration, tuning or trimming. To minimize such error induced distortion and avoid over-design, the precision of the reference voltage buffer should be 1 bit less than the required resolution of the entire ADC. Moreover, to prevent package-inductance-induced oscillation, stabilizing the reference voltage in very-high-speed operation requires purely on-chip solution. With small overhead on the MDAC, both the proposed on-chip compensation techniques have adequate performance and feature simple in implementation.

For the static errors, positively offseted reference voltage only lengthens the conversion curve and results small lost in the SNR, whereas the negatively one clipped the signal amplitude and induced spurious tones that limits both ENOB and SFDR. Post-fabrication calibration to this error is possible by using switched-resistor bank. The random-noise modulation is also classified as static, which can be approximately considered as one ingredient of the MDAC input-referred noises. Both DC offset and random noise can limit the full-scale signal swings and they are become very critical in low-voltage design.

Acknowledgments

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