NOVEL LOW JITTER MULTI-PHASE CLOCK GENERATION SCHEME FOR PARALLEL ANALOG-TO-DIGITAL CONVERSION SYSTEMS

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ABSTRACT

This paper presents a detailed analysis of low-jitter clock generation techniques for time-interleaved (TI) analog-to-digital converters (ADC). In additions, a novel low-jitter, multi-phase non-overlapping clock generator will be proposed. The clock generator can provide various clock phases for TI ADCs or even general analog-to-digital (A/D) conversion path (e.g. TI decimation filter) and has the advantages of being insensitive to timing mismatches and clock duty cycles inaccuracies, having a simple and highly robust architecture such that the clock generator can be generalized for an arbitrary number N of time-interleaved (TI) paths. Simulation results using Hspice are provided to verify the effectiveness of the proposed clock generator.

Keywords –Multi-phases, clock generator, ADCs, time-interleaved (TI), timing mismatches, clock jitter

1. INTRODUCTION

High-speed sampled-data systems are experiencing an increasingly demand from the present telecommunication systems, as well as, from other signal processing applications, like for example, the single-chip CMOS receiver [1,2], the digital oscilloscope and RGB-LCD display conversion [3]. Time-Interleaved (TI) architectures are one of the effective solutions to the high-speed sampled-data systems, but they suffer from periodic timing skew that produces modulation images at frequency locations of multiples of f_s/M (f_s-overall sampling rate, M-period of timing skew), which are caused by timing mismatches in different time-interleaved paths [4]. These images will severely affect, especially, the dynamic range of TI-sampled data systems in very high-speed applications. As the sampling frequency increases beyond 100MHz, the design of a low-jitter, non-overlapping clock generator becomes a critical task to ensure a satisfactory performance of such high-speed systems.

Various techniques had been reported in the literature to produce low-jitter sampling clocks [3-9]. Among them the more accurate technique comprises the utilization of precise clock edges, such as those from master clock [3-5,7-9] to reduce the timing skew. In this paper, a novel low-jitter multi-phase non-overlapping clock generator will be proposed, which can be directly applied in parallel A/D conversion path (e.g. TI ADCs and decimation filters). It presents significant advantages due to the simple circuit architecture and the high robustness that allows its extended operation to multi-phase with a low hardware cost.

2. CLOCK EDGES REQUIREMENTS

The sampling instants of sampled-data systems are defined either at the rising or falling edges of the sampling clock, thus implying that the clock edges inaccuracy would be directly related to the timing jitter. Considering, for example, an SC TI sample-and-hold (S/H) circuit from an A/D conversion path with generalized any number of paths [10], as shown in Fig. 1(a). As it is common in SC circuits, they usually require multi-phase non-overlapping clock signals $\phi_1 \ldots \phi_N$ and $\phi_1' \ldots \phi_N'$ to control the analog switches. Thus, in order to minimize the effect of signal-dependent charge injection and clock feedthrough errors [3] in the sampling capacitors $C_1 \ldots C_N$, the switches controlled by pre-phases $\phi_{1p} \ldots \phi_{Np}$ will be opened slightly earlier than the post-phases $\phi_1 \ldots \phi_N$, which means that the falling edges of the pre-phases should appear slightly earlier than that of the post-phases as shown in Fig. 1(b). On the other hand, for certain applications with higher accuracy, the rising edges of the pre-phases could be placed also slightly earlier than that of post-phases to further suppress the charge injection errors (with small loss on the available settling time of the opamp) [11].

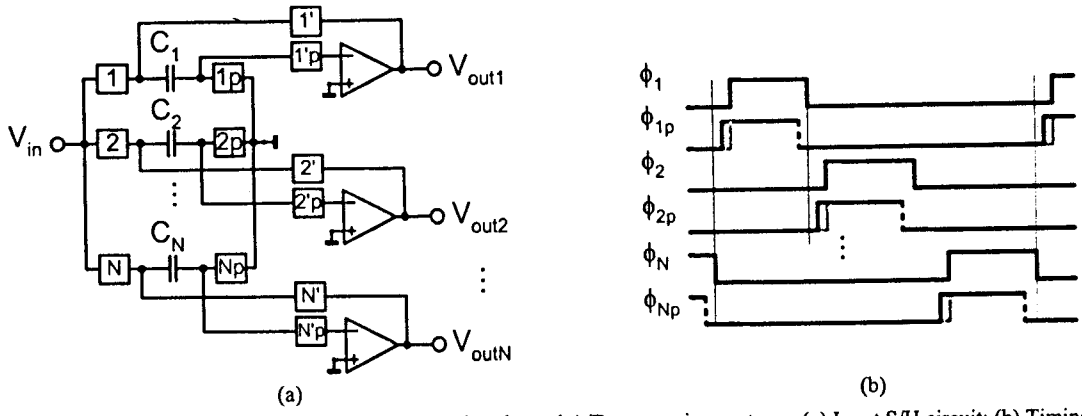

Fig. 1: SC sampled-and-hold circuits used in time-interleaved A/D conversion systems: (a) Input S/H circuit; (b) Timing-diagram

However, for better settling of the opamps, both phases can rise together as shown in all edges, in gray-color, in Fig. 1(b). Inaccurate sampling clock edges produce periodic timing skew with period M=N and, consequently through this arrangement, the **falling edges** of the **pre-phases** would become the critical edges to be controlled for avoiding timing skew in **A/D conversion paths** [3].

3. A NOVEL LOW-JITTER MULTI-PHASE CLOCK GENERATOR

According to the previous mentioned analysis a novel clock generation scheme for low-jitter, multi-phase non-Overlapping clock phases has been developed. This platform is for applications of TI A/D conversion systems (including decimators). Fig. 2 shows the block and timing diagrams of the proposed clock generators, which relies on accurate control of critical clock edges to reduce timing-skew errors for A/D conversion systems. On the other hand, Fig. 3 exhibits the clock generator containing the following building blocks:

A. Master-slave D-flip-flop with master output

Fig. 3(a) shows a master-slave D-flip-flop (DFF) with an additional master output that is extracted from the master latch. With such arrangement the master (M) output signal always leads the slave (Q) quadraturely.

B. Self-starting mod-N ring counter

The self-starting mod-N ring counter is designed to provide shifted negative pulses, which serve as envelopes of various multi-phase clock signals to ensure a non-overlapping operation. Fig. 3(b) shows an example of a design of self-starting mod-4 ring counter, where dummy gates are used to balance the loading conditions of Q and M outputs.

C. Edge Decision Block (EDB)

Since for A/D converters (or decimators) the critical sampling edges are on the falling edges of the pre-phases, these falling edges will be "assigned" by the rising edges of an accurate clock (pre/post-clk, delay version of master clock by d_0 and d_0+d_{pre} respectively), as it is presented in Fig. 2(b) together with the resulting clock phase outputs ϕ_{mp}/ϕ_m (m=1...N).

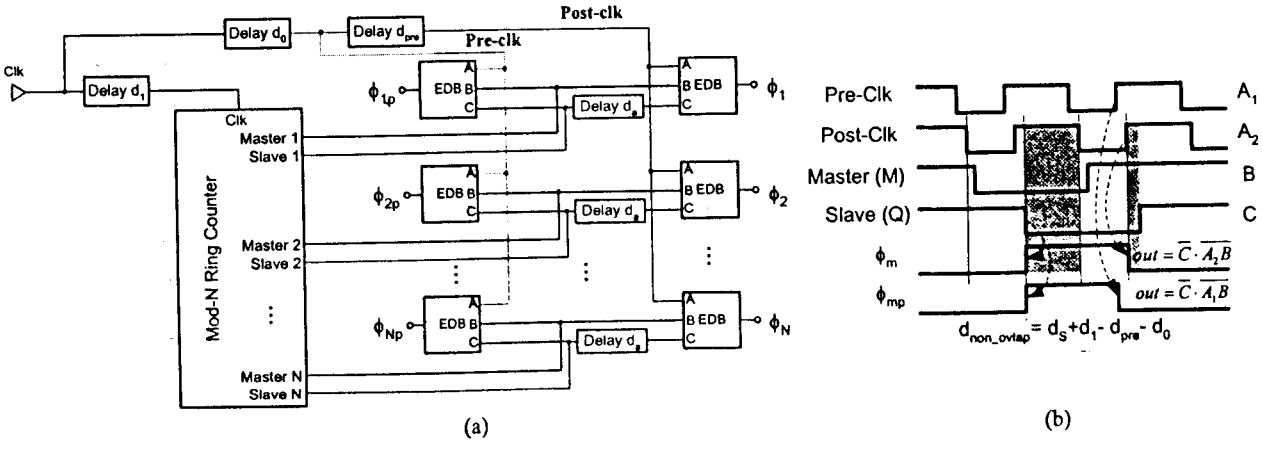

Fig. 2: Proposed (a) block and (b) timing diagrams of the low-jitter multi-phase clock generator in TI A/D conversion

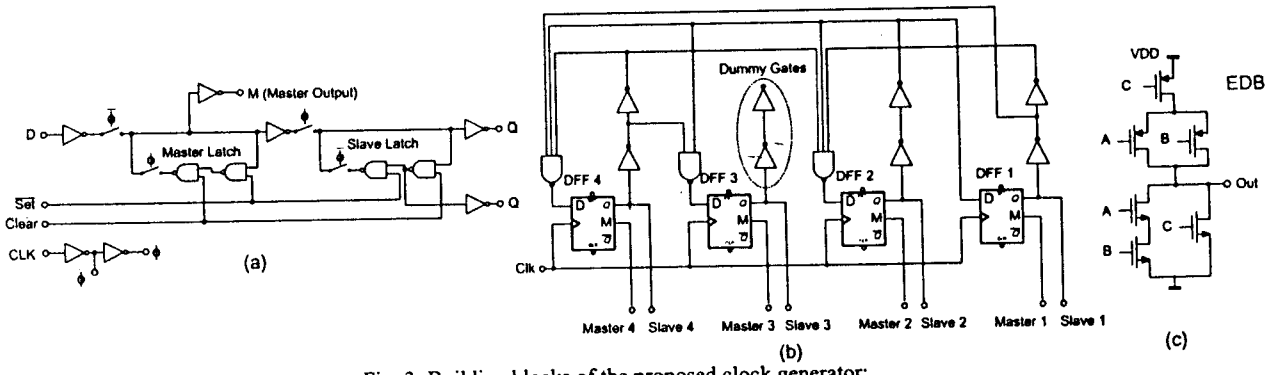

Fig. 3: Building blocks of the proposed clock generator:
(a) Master-slave DFF with master output; (b) Self-starting mod-4 ring counter; (c) Edge Decision Block (EDB)

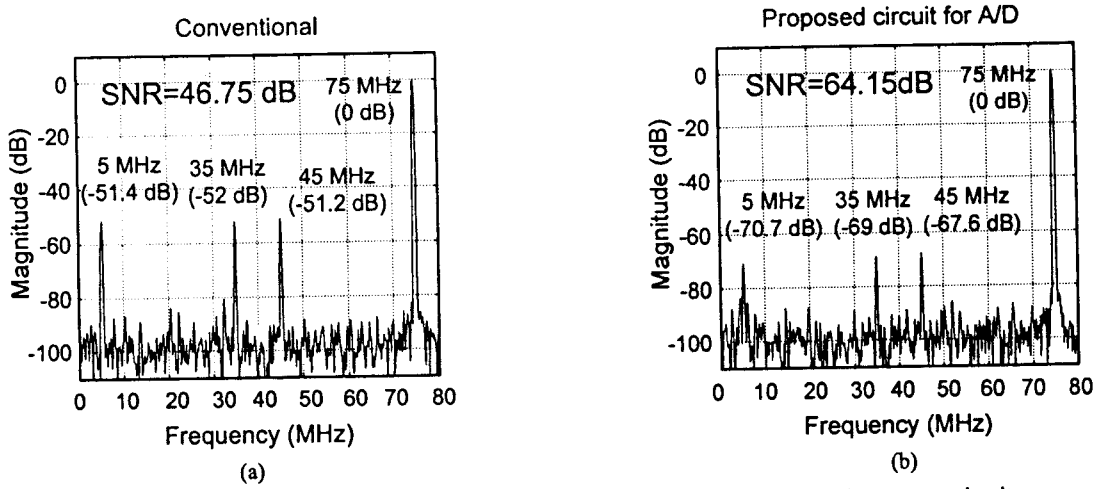

Fig. 4: Hspice FFT simulation results for the: (a) conventional; (b) proposed clock generator circuits

However, this assignment is not possible, as it can be verified for example in the shaded area of Fig. 2(b), where the post-clk signal is equal to 1 and the slave (Q) is 0 in both areas while the output ϕ_m is dissimilar. In order to identify separately these two regions a master output M from the DFF serves as a boundary between the shaded areas. According to the assignment of alphabetic letters shown in the figure, the logic function that implements the desired output is given by

$$out = \overline{C} \cdot \overline{AB} \qquad (1)$$

and the circuit diagram shown in Fig. 3(c), called "Edge Decision Block" (EDB), can be used to implement such a logic function. Also, the function of all shaded delay block d_a in Fig. 3 is used to provide a delay between the rising edges of pre- and post-phases to further reduce charge injection errors as discussed in previous section. The amount of non-overlapping time delay is also shown in bottom of Fig. 2(b), while the delay between the falling edges of pre-phases and post-phases can be easily determined in Fig. 2(b) as d_{pre}.

5. SIMULATION RESULTS

In order to verify the effectiveness of the proposed clock generator, a 4-phase version of the clock generators were simulated with Hspice with the master clock frequency set at 160 MHz (also the overall sampling rate).

The designed clock generators are used to drive the switches in the TI S/H circuits to sample a 75 MHz sinusoidal signal with the overall sampling frequency of 160 MHz. Fig. 4(a) shows the FFT output spectrum for the S/H circuits that are driven by the 4-phase version of the conventional feedback type clock generator from [12] that has no control over clock edge accuracies. The spectrum shows 3 mismatch-induced image tones appearing at frequency 5, 35, 45 MHz, respectively, and only 46.75 dB SNR is achieved, corresponding to 13 ps timing mismatches by the formula derived in [4]. Fig. 4(b) shows the corresponding spectrum with the proposed clock generator the image tones are effectively reduced with an SNR of 64.15 dB (less than 2 ps timing mismatches), corresponding to 17~19 dB improvement.

Monte Carlo Simulations are the effective means to evaluate the effect of timing jitter due to its statistical nature. To evaluate the timing skew produced in the proposed clock generator circuits, 100-run Monte Carlo simulations were performed and the clock edges timing

errors are calculated subjected to the process mismatches (time-interleaved path = 4). All the timing errors in the Monte Carlo simulations are found as deviations from the corresponding nominal timing differences, i.e. the timing skew. Table 1 is a summary of the results. From the results of the Monte Carlo simulations the standard deviations of the timing skew can be as large as 12 ps in the conventional clock generator circuits. With the proposed clock generation techniques the standard deviation of timing skew has been effectively reduced to 1.84 ps, reducing the timing skew produced by process mismatches by as large as 85%. Notice that only the timing-jitter in the shaded boxes of the table (which is the falling edges of the pre-clk) required to accurately control, as mentioned in the previous sections that the critical edges of TI ADCs are on the pre-clk falling edges.

Table 1: Summary of Monte Carlo simulations for the various clock generators[1]

	Clock Generator	Conventional	Proposed A/D
Standard Deviations	Post-Clk Rise	12.9 ps	9.5 ps
	Pre-Clk Rise	12.8 ps	8.6 ps
	Post-Clk Fall	12.5 ps	1.82 ps
	Pre-Clk Fall	12.1 ps	1.84 ps

[1]Shaded boxes denote the edges that are critical to avoid the effects of timing skew.

6. CONCLUSIONS

A thorough generalized analysis on multi-phase clock generation techniques to reduce timing skew effects in parallel or time-interleaved A/D conversion systems has been presented. Then, a novel low-jitter, multi-phase non-overlapping clock generator is proposed. The proposed clock generator can provide clock phases to TI ADCs or decimation filters. Transistor level Simulations are also provided to verify the effectiveness of the proposed clock generation techniques. Hspice simulation results shows 17 dB improvement in SNR (with jitter reduced from 13 ps to 2ps) compared with the conventional clock generator as verified by the Monte Carlo and FFT analysis of the simulated results.

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