N-PATH MULTIRATE SIGMA-DELTA MODULATOR FOR HIGH-FREQUENCY APPLICATIONS

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ABSTRACT

An *N*-path multirate architecture for implementing sigma-delta modulator (SDM) is proposed in this paper. The replacement of the first integrator in the *N*-path structure can relax the speed requirements of the opamps in the first stage. The use of comb filters in that integrator can also alleviate various mismatch effects. Comparison with conventional and other multirate SDM architectures is also presented. Simulation results show that the proposed architecture has several advantages when compared with previous implementations, such as low sampling frequencies, average performance for arbitrary *N* and reduced mismatch sensitivity between *N* paths.

1. INTRODUCTION

The utilization of oversampling analog-to-digital modulators to handle high-frequency signals is one of the trends today in modern analog IC design [1]. However, the major limitations for the use of SDMs in high-frequency applications, such as wide-band and video signal, are the internal clock rate and the op-amp bandwidth.

Because the critical performance of a second-order SDM is determined by the first stage [2,3], the design of the first integrator becomes a very important and critical issue. However, it is difficult to design an integrator operating at high sampling rate over 100MHz. Therefore, a multirate technique has been recently proposed for SDMs, such as Multirate-Multibit SDM (MM-SD) and Multirate Single-bit SDM (MS-SD), to overcome the previous mentioned obstacles [4,5]. For a second-order SDM, it has been proposed to decimate the output signal and then feedback it to the first stage which will be working at a low sampling rate. Afterwards, the signal will be interpolated for the second stage. This means that, the first stage operates at low sampling rate and the second remains at higher sampling rate. An analysis method that relies on the translation of the multirate modulator into a single-rate system using polyphase decomposition can also be found in recent applications [6]. For high-order SDM, Multirate Cascade SDM (MC-SD) can provide no decimated feedback to the analog circuitry working at the low sampling rate [7].

However, for the models MM-SD and MS-SD, stability is the major problem because of the introduction of distortion and aliasing to the Noise Transfer Function (NTF) during decimation and interpolation. The existence of multi-bit Digital-Analogue Converter (DAC) will also affect the linearity in MM-SD. Besides that, for all models, the digital operations will offer an extra complexity in terms of circuitry with drawbacks that limit the practical utilization of such modulators.

An alternative type of architecture, Time-Interleaved SDM (TIM), can also be found in [8], which is derived from the combination of the architecture of a block digital filter together with *N* interconnected low-speed SDMs to obtain high signal-to-noise ratio (*SNR*). *N*-path architecture allows the processing of a signal sampled at frequency *NF* by *N* subsystems operating at frequency *F*. But, because of the intrinsic parallel nature, applying pure *N*-path architecture directly in SDM will produce a re-sample effect and will push noise into the baseband which will increase the noise floor and reduce *SNR*. Furthermore, this type of converters is subject to the mismatch effects between *N* paths. In [9], the effect of coefficient mismatch on the performance of a block digital filter is studied where it is shown that due to mismatches, the overall structure becomes time-varying and hence aliasing will be present. It was also emphasized that those portions of the spectrum around $2\pi i/N$ (i = 1, 2, ..., N) would be folded back into the baseband.

In order to overcome the previous mentioned drawbacks, it is presented in this paper a new architecture that uses an *N*-path integrator in the first stage, thus eliminating the aliasing caused by sample rate conversion, due to its perfect reconstruction nature. Meanwhile, a comb filter is applied in the first stage to cancel the re-sample effect and to alleviate the mismatch effects between *N* paths.

The overall architecture proposed is running on 1-bit and is totally analogue to prevent the usage of DAC and digital circuitry. In the following sections, a combined structure for the comb filter and *N*-path integrator will be introduced. Simulations show that the proposed SDM can achieve good performance on either *SNR* or mismatch-insensitivity.

2. *N*-PATH MULTIRATE MODULATOR

The linear model of the *N*-path multirate SDM is shown in Figure 1, where the first stage is composed of two parts, a comb filter and an *N*-path integrator. In order to compensate

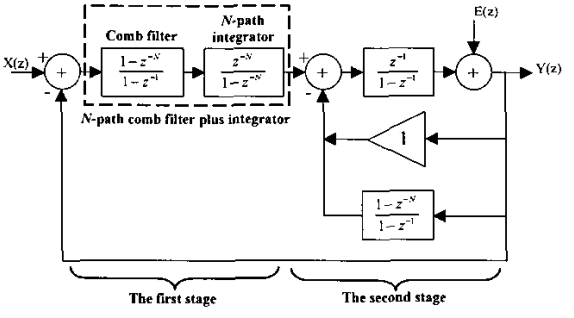


Fig.1 N-path multirate second-order sigma-delta modulator

the influence of the delays caused by the N-path integrator, an additional comb filter is inserted into the inner feedback loop of the second stage.

By carefully tracing through the model, the output of the modulator can be described as,

$$Y(z)=\frac{z^{-1}}{1-z^{-1}}\cdot\left\{\frac{1-z^{-N}}{1-z^{-1}}\cdot\frac{z^{-N}}{1-z^{-N}}\cdot[X(z)-Y(z)]-\left[1+\frac{1-z^{-N}}{1-z^{-1}}\right]\cdot Y(z)\right\}+E(z) \tag{1}$$

that will lead finally to,

$$Y(z)=z^{-(N+1)}X(z)+(1-z^{-1})^2E(z) \tag{2}$$

which is a typical transfer function of a second-order SDM. However, its first stage is operating at low sampling rate so as to relax the design requirements and to reduce the power consumption which allows the use of CMOS op-amp in the structure. Because the performance of a second-order SDM depends more critically on the first integrator, keeping the second integrator at a higher sampling rate doesn't affect the performance and can even simplify the circuit.

As described in [9], the effect of coefficient mismatch on the performance of a block filter causes those portions of the spectrum around $2\pi i/N$ (i = 1, 2, ., N) getting folded back into the baseband in order to reduce SNR. In N-path filter version, the aliased components $A(z)$ can be described as,

$$A(z)=\frac{1}{N}\sum_{i=1}^{N-1}X(zW^i)\sum_{j=0}^{N-1}z^{-(N-1-j)}\sum_{k=0}^{M_j-1}a_{jk}h_{jk}z^{-k} \tag{3}$$

where M_j is the order of each FIR term in a sub-filter $H_j(z)$, a_{jk}'s are the mismatch ratios and h_{jk}'s are the ideal coefficients.

In other words, aliased components of the input spectrum $X(zW^i)$ will first get multiplied by the productions of the mismatch ratios and the ideal coefficients and then folded back into the baseband.

As it is known, comb filter is a good solution to eliminate the major aliased components by placing the zeros on $f_s/2N$. Therefore, in the proposed SDM, the preceding comb filter alleviates the mismatch effects on the N-path integrator. On the other hand, in order to lower the sampling rate for the comb filter, this is combined into an N-path integrator, as shown in Figure 2(a) and 2(b). Note that in Figure 2(b), the number of paths, N, is equal to 4 for illustration purpose. In Figure 2(b), all the summation and the integration is done among downsamplers and upsamplers. That is to say, the combined structure, N-path comb filter plus integrator, operates at the low sampling rate.

3. CIRCUIT ARCHITECTURE

3.1. N-path comb filter plus integrator

Figure 3 shows the SC realization of one path of the 4-path comb filter plus integrator. The downsamplers and upsamplers are implemented by the switched-capacitor elements with a variety of clock phases.

The integrator uses two signal-sampling paths that implement double-sampling. They allow that the charge transfer slot-time that is available to the opamps is almost equal to the clock period and the input signal sampled on both clock phases.

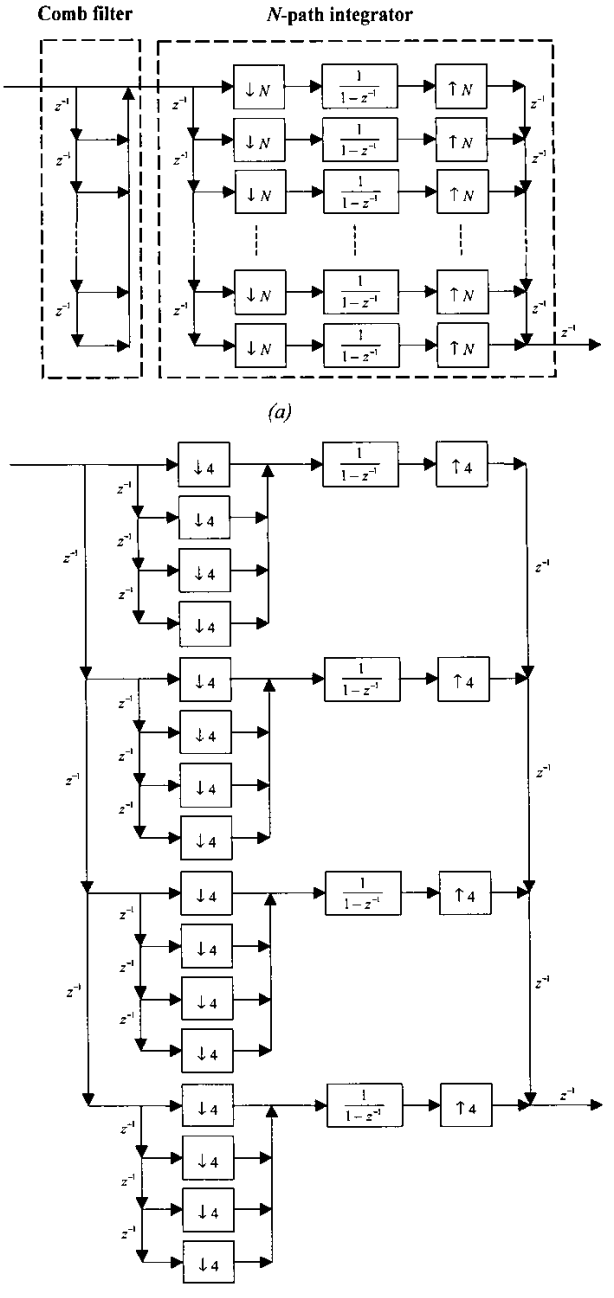


Fig.2 (a) A comb filter followed by an N-path integrator
(b) The combined structure: N-path comb filter plus integrator with N=4

3.2. Sampling rate and clock phases

In accordance with the specifications given in CCIR-601 which describes studio digital video coding, the chrominance signals (C_r and C_b) are sampled at a frequency of 6.75MHz (3MHz × 2.25) and are coded with 8-bit PCM words. Herein, we have chosen an oversampling rate (OSR) of 36 (3MHz ×

2.25 × 32 = 216MHz) because 32 is a power of 2, for easily design the decimator in the following process. Theoretically, if *OSR* = 36, it will give a maximum of 70dB *SNR*, equivalent to 11.5-bit PCM words.

In our circuit, phase 0 is operating at 216MHz; Phases 1A, 1B, 1PA-4PA and 1PB-4PB are at 27MHz. For phases 1A and 1B operating at 27MHz, the charge transfer slot-time for the opamps can reach 13.8ns.

3.3. Fully differential balanced circuit

A fully differential balanced circuit for the 4-path multirate second-order SDM has been designed and its behavioral simulation is demonstrated by using SWITCAP2 [10-12].

The fully differential balanced configuration can reduce the effects of charge injection via the switches (the switch-induced errors), improves the power supply noise rejection and common mode rejection (dc offset) and increases the dynamic range. Beyond the advantages mentioned above a fully differential configuration also provides additional design flexibility due to the availability of signals of both signs. Negative or positive gain can simply be realized by reversing the input or output signal pair.

4. SIMULATION RESULTS

Figure 4 shows the Signal to Noise plus Distortion Ratio (*SNDR*) of the 4-path multirate second-order SDM compared with the conventional second-order SDM. These curves were obtained by the simulation with Matlab [13], where the *OSR* of the conventional second-order SDM is 36. It can be observed that they show a good matching when compared with the conventional SDM. And it indicates that the peak *SNDR* for *N*-path multirate SDM is 50dB (equivalent to 8-bit PCM).

In Figure 4(*a*), the re-sample effect and aliasing cause the *SNDR* to drop down either when applying pure *N*-path architecture or when no comb filter is applied in *N*-path multirate SDM.

Figure 4(*b*) shows comparison with MM-SD, MS-SD and 2-2 MC-SD (fourth-order SDM). Because *SNDR* of MM-SD, MS-SD and MC-SD are determined by the *OSR* of the first stage (OSR_1) [4-7], apparently their performances become deteriorated when *N* increases. On the other hand, *SNDR* of the proposed SDM is determined by the *OSR* of the second stage (OSR_2). Hence, the performance of the *N*-path multirate second-order SDM has no degradation.

The output spectrum from the circuit for 4-path multirate second-order SDM and that for the conventional second-order SDM are compared in Figure 5 with -10dB input amplitude and without mismatch effects. It shows that the performance of the proposed SDM is similar to the one of the conventional SDM.

When mismatch exists in the *N*-path integrator, the aliasing causes a flattening of the noise floor in the baseband sitting around -80dB, as shown in Figure 6. Furthermore, multirate SDM tends to generate limit cycles at frequencies of $f_s/2N \pm if_{in}$ where f_{in} is the input frequency. Due to mismatch, these limit cycles will also fold back into the baseband and cause tones at if_{in} as if they were harmonics of the input frequency f_{in}. Note that these tones are originated from the time-varying nature of the structure rather than its nonlinearity. When a comb filter is applied, because of the existence of notches at $f_s/2N$, the noise

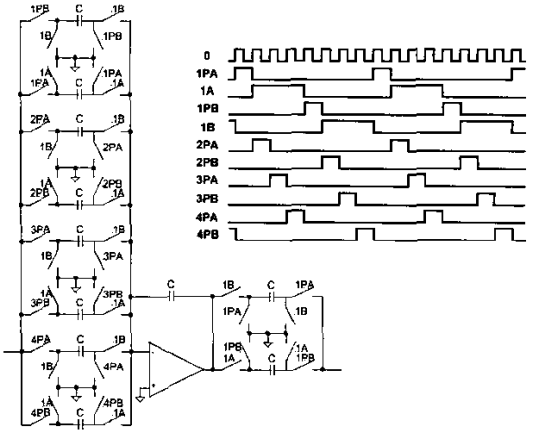
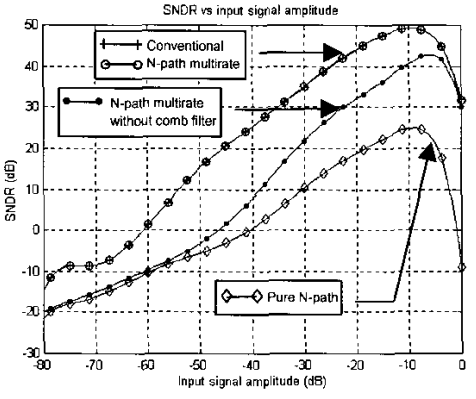
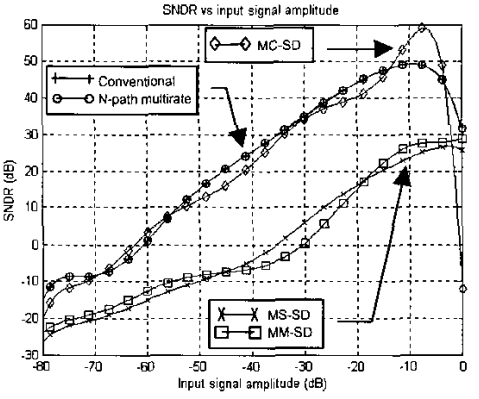


Fig.3 One path of the 4-path comb-filter plus integrator



(a)



(b)

Fig.4 Simulated SNDR for various SDM, (N=4, OSR_1=9, OSR_2=36)
(a) Comparison with Pure N-path architecture
(b) Comparison with MM-SD, MS-SD, MC-SD

floor in the baseband shows an apparent improvement in which the aliased component is negligible, as well as, the tones at if_{in}.

In order to illustrate the mismatch effects, Monte Carlo simulation for 200 samples has been performed on the proposed SDM. Typically, the mismatch ratio for capacitors can be controlled within 0.4%. Herein, supposing that the mismatch ratio is described by Gaussian Distribution and supposing that the standard deviation σ is equal to 0.2%. Then the simulation results from Figure 7 show that $\Delta SNDR$ are less than 0.97dB within σ, 1.33dB within 2σ and 3.42dB within 3σ, respectively. These indicate that the circuit is mismatch-insensitive.

5. CONCLUSIONS

N-path multirate sigma-delta modulator has been presented in this paper. The modulator provides low sampling rate in the first integrator meanwhile achieving performance similar to the conventional modulator. For stability, mismatch-free and delay compensation, comb filters have been applied in the first stage and in the inner loop of modulator. The comb filter in the first stage alleviates the major mismatch effects on the *N*-path integrator. A Monte Carlo simulation has verified the efficiency of this comb filter. Furthermore, the comb filter is combined with the *N*-path integrator to form an *N*-path comb-filter plus integrator and allow the comb filter and the integrator to operate in low sampling rate. Moreover, another advantage with the *N*-path multirate sigma-delta modulator is that for arbitrary *N*, the realization of *N*-path multirate sigma-delta modulator is usually an easy and straightforward procedure.

6. REFERENCES

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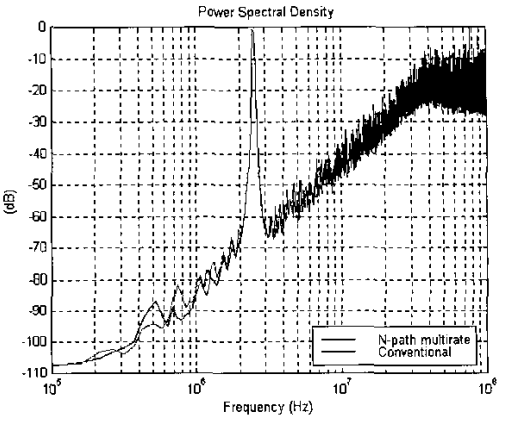

Fig.5 ***Output spectrum for a -10dB 2.5MHz input sine-wave at 216MHz sampling frequency***

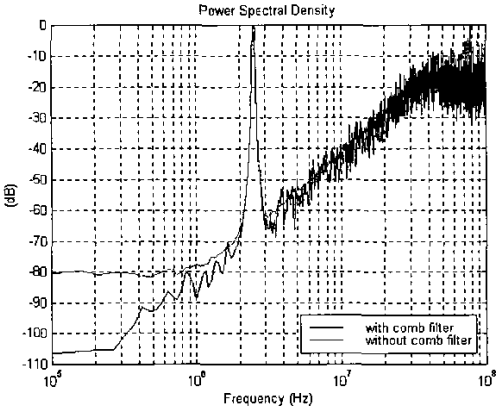

Fig.6 ***Output spectrums with 0.4% coefficient mismatch by using comb filter versus no comb filter***

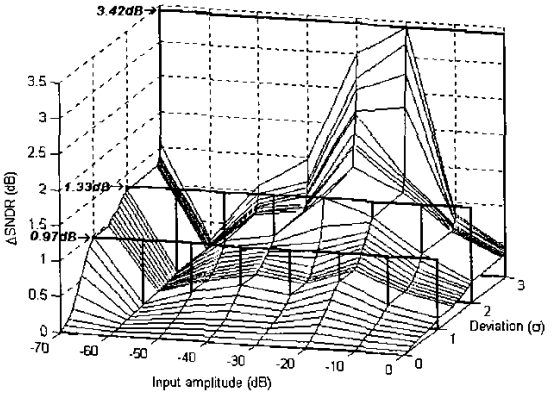

Fig.7 ***Monte Carlo simulation shows $\Delta SNDR$ within different deviation σ, 2σ and 3σ, where σ=0.2%***