Source-Follower-Based Bi-quad Cell for Continuous-Time Zero-Pole Type Filters

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ABSTRACT

Presented is a novel source-follower-based (SFB) bi-quad cell suitable for realizing continuous-time zero-pole type filters. Unlike the conventional SFB bi-quad cells that can only realize complex poles, additional complex zeros can be synthesized in the proposed one, by adding two feedforward capacitors. A 4th-order Chebyshev II fully differential low-pass filter prototype was fabricated in a 0.18-μm CMOS process. The achieved bandwidth is 2.75 MHz with +5 dBm in-band IIP3 and -1 dB gain. The power consumption is 3 mV at a 2-V supply.

I. INTRODUCTION

In most modern wireless receivers (RXs), the quality of channel-select filter directly influences the RX overall dynamic range. Among the main specifications of on-chip channel-select filters [1], the dependence of power and linearity addresses impact on the performance of several continuous time filter structures, such as Active-Gm-RC [2], Active-RC [3] and Gm-C [4] filters. Recently, D'Amico has proposed an alternative approach: source-follower-based (SFB) bi-quad cell for continuous time filters [5], served as an excellent choice to maximize the power efficiency while maintaining low nonlinearity.

In the case of magnitude approximation of a filter transfer function, the most popular low-pass functions are the following: Butterworth, Bessel, Chebyshev I, Chebyshev II and Elliptic function [6]. In terms of the combination of zeros and poles in filter transfer function, one could categorize filters in two classes: (1) all-pole type of filters, for example, the Butterworth, Chebyshev I and Bessel filter; (2) zero-pole type of filters including the Chebyshev II and Elliptic filters. In this paper, we deal with the latter type of filters which can achieve a shaper cutoff characteristic.

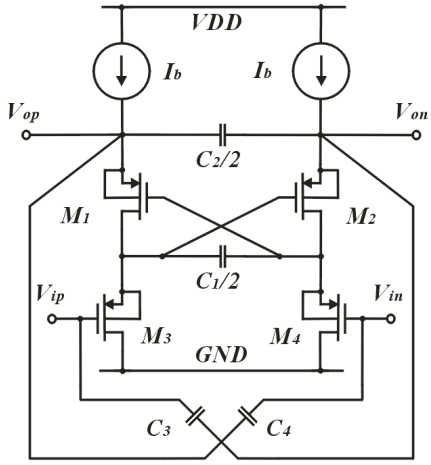

Fig. 1. Proposed SFB low-pass bi-quad cell with poles and zeros.

SFB bi-quad cell which is proposed by D'Amico [5] can only implement one of all-pole type of filters, low-pass Bessel filter. Thus, in this paper we present novel sourced-follower-based bi-quad cell for designing zero-pole type of filters.

The paper is organized as follows. In section II, the proposed bi-quad cell is described. The 4th-order Chebychev II fully differential low-pass filter using proposed cell is shown in section III. The experimental results are presented in section IV, followed by conclusion in section V.

II. PROPOSED BI-QUAD CELL

Figure 1 shows the implementation of the proposed low-pass bi-quad cell which presents a PMOS-based single-branch fully differential structure. The two in-phase feedforward capacitors C_3 and C_4 implement the extra complex-conjugate zeros in addition to its complex poles such that it can befit zero-pole type of filter synthesis. The PMOS transistors are of

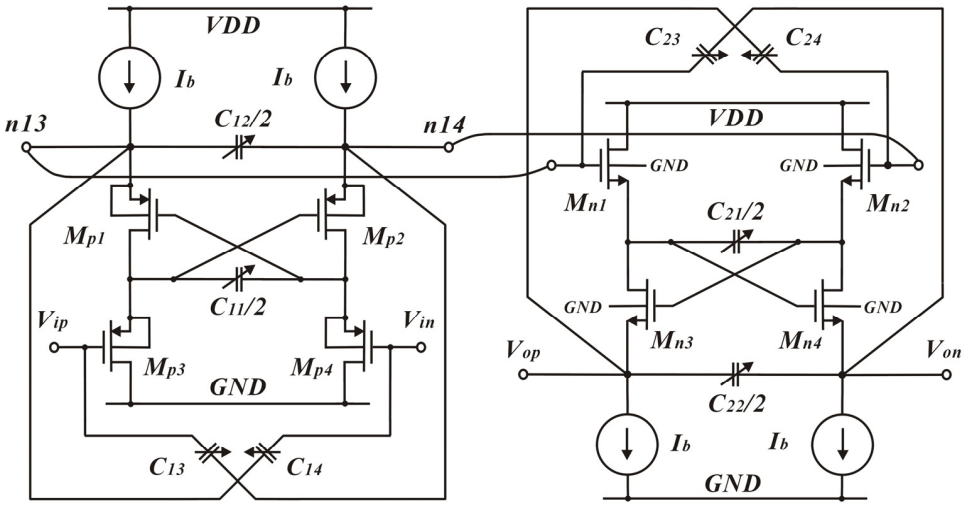

Fig. 2 Proposed and implemented 4th-order fully differential SFB active filter

the same size and current, so as their transconductance, i.e., $g_{m1} = g_{m2} = g_{m3} = g_{m4} = g_m$. In the following analysis, the PMOS output conductance is assumed to be negligible with respect to the transconductance, and the transistor's parasitic capacitors are not assumed to be non-dominated. Let $C_3 = C_4 = C_f$, the small signal analysis gives the low-pass bi-quad cell transfer function as follows,

$$H(s) = \frac{\frac{C_f}{C_2 + C_f}(s^2 + \frac{g_m^2}{C_1 C_f})}{s^2 + s(\frac{g_m}{C_2 + C_f}) + \frac{g_m^2}{C_1(C_2 + C_f)}} \tag{1}$$

where C_1 and C_2 are the total grounded capacitance at the M3 and M4 transistor's sources and at the output nodes, respectively. C_f is the total forward capacitance at the gate of transistor M3 and at the source of M2, and C_4 is that for M4 and M1. The filter parameters are summarized as bellow:

$$\omega_0 = 2\pi f_0 = \frac{g_m}{\sqrt{C_1(C_2 + C_f)}}, \quad \omega_z = 2\pi f_z = \frac{g_m}{\sqrt{C_1 C_f}},$$
$$Q_p = \sqrt{(C_2 + C_f)/C_1}, \quad K = 1 \tag{2}$$

where K is the DC gain, f_0 is the pole frequency, f_z is the zero frequency and Q_p is the quality factor of pole. From (2), ω_z forms out-of-band notch in zero-pole type filter.

III. Filter Design and Implementation

A cascade of two proposed cells has been exploited to implement a 4th-order fully differential low-pass filter with Chebychev II approximation, and is shown in Fig. 2. It is realized in a 0.18-μm CMOS technology with a 2-V supply. The 1st cell is structured by PMOS type, while the 2nd one is of NMOS type. In the 1st cell, all transistors with a back-gate connection of the PMOS devices are designed with the same size and the same current level. Thus, they have the same transconductance gm. However, the zero characteristic in the transfer function of the 2nd cell is affected by the NMOS (Mn1&Mn2) back-gate transconductance. While the NMOS (Mn1&Mn2) back-gate transconductance is not negligible with respect to the transconductance, the low-pass bi-quad cell transfer function is derived as Eq. (1), shown at the bottom of this page, where C_1 and C_2 are the total grounded capacitance at the Mn1 and Mn2 transistor's sources and at the output nodes, respectively. C_f is the feedforward capacitor. The NMOS (Mn1&Mn2) transconductance and back-gate transconductance are g_{m1} and g_{mb1}, g_{m2} and g_{mb2} are the NMOS (Mn3&Mn4) transconductance and back-gate transconductance, respectively.

The s term is equal to zero in the numerator of the equation (1), and this means Q_z which is the quality factor of out-of-band zero is infinite. However, because the NMOS (Mn1&Mn2) back-gate transconductance is not negligible, the relation of g_{m1}, g_{mb1} and g_{m2} can be written as follows,

$$H(s) = \frac{\frac{C_f}{C_2 + C_f}(s^2 + s\frac{(g_{m1} + g_{mb1} - g_{m2})}{C_1} + \frac{g_{m1} g_{m2}}{C_1 C_f})}{s^2 + s(\frac{g_{m2} + g_{mb2}}{C_2 + C_f} + \frac{(g_{m1} + g_{mb1} - g_{m2})}{C_1}) + \frac{(g_{m2} + g_{mb2}) g_{m2} + (g_{m2} + g_{mb2})(g_{m1} + g_{mb1} - g_{m2})}{C_1(C_2 + C_f)}} \tag{3}$$

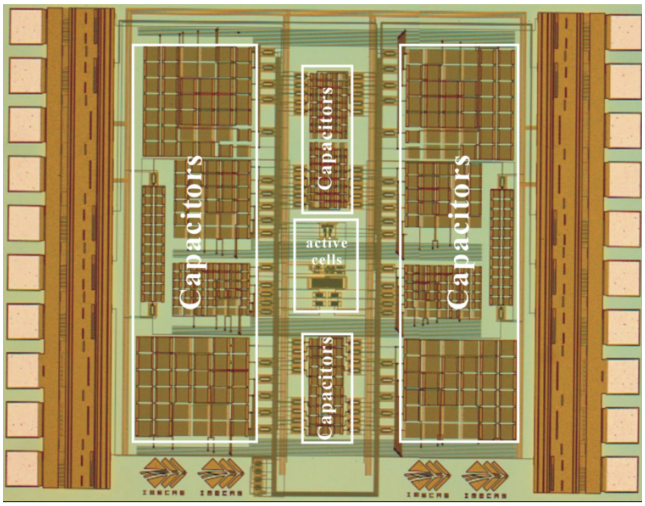

Fig .3 Die photograph of proposed low-pass filter

$$g_{m1} + g_{mb1} = g_{m2}\,. \tag{4}$$

Active core circuits of proposed bi-quad cell are not tuned to avoid filter transfer function distortion. Instead, capacitor banks are employed for filter's frequency tuning. Arrays of 4-bit tuning capacitor are used to compensate process parameter tolerances. W and L of the switches are optimized to introduce a minimal error in the frequency response of the filter. The proposed low-pass filter with Chebychev approximation has been fabricated using SMIC 0.18-µm CMOS process. Its die micrograph is shown in Fig. 3. The chip performance was measured by chip-on-board. S-parameters of the fabricated low-pass filter are measured using Agilent N5230A network analyzer. Fig.4 shows the measured frequency response of the filter, measured cut-off frequency is 2.75 MHz. The transfer function of filter has two out-of-band notch frequencies, 9.3 and 15 MHz, as designed. The NMOS back-gate transconductance makes the gain loss of the 2nd cell (NMOS-based) decreasing to 1 dB. The gain loss can be avoided with a back-gate connection of the single NMOS transistor in a triple-well CMOS process.

IV. Measurement Results

The chip area including pads is 1mm × 1.3mm. The area occupation has been limited by the low-density capacitors (1 fF/mm^2). Thus, the chip area can be significantly reduced when high-density capacitors are available. The capacitors include arrays of 4-bit tuning capacitor for compensating the process parameter tolerances. It can be incorporated with a g_m-C tuning engine for automatic calibration. Figure 5 shows the measured result of a two-tone test with 1.75 and 2.25 -MHz inputs (with a power of -16 dBm). The achieved in-band IM3 is around -40 dB. This corresponds to an in-band IIP3 of +5 dBm. The linearity has been evaluated also in terms of HD3, which is -46.3 dB with 350-mV$_{pp}$ input amplitude; the result is given in Fig. 6. The total input

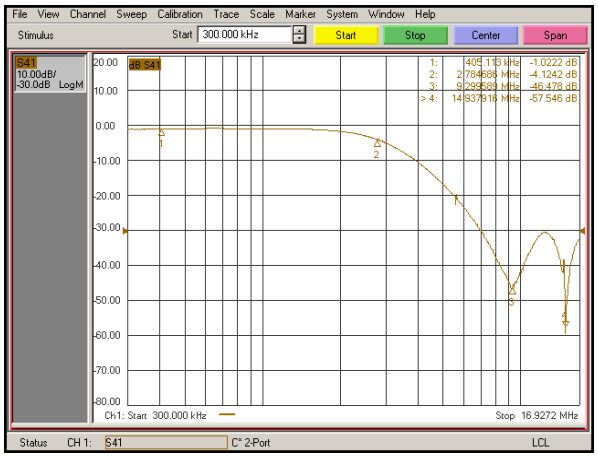

Fig. 4. Measured filter frequency response

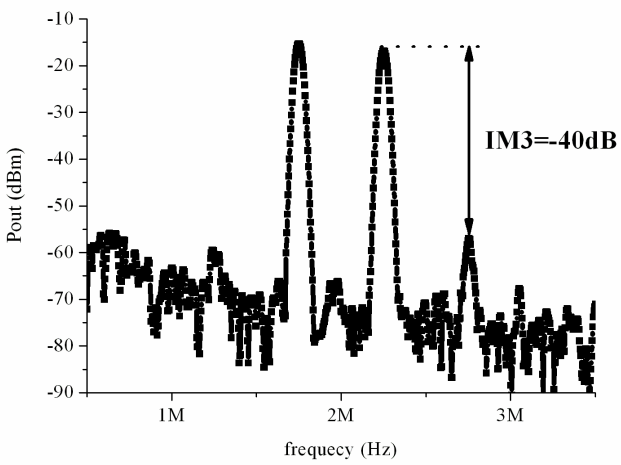

Fig. 5. 2-tone test for In-band IM3 measurement

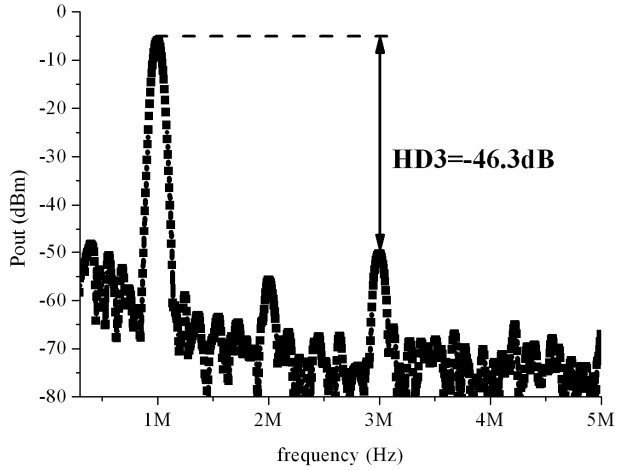

Fig. 6. Single-tone test for In-band HD3 measurement

inferred noise voltage is about 70 µV$_{rms}$. Comparing with [5], the dynamic range is worse due to need of a test buffer. The current consumption is 1.5 mA at a single 2-V supply. The filter characteristics are summarized in TABLE I.

TABLE I

SUMMARY OF FILTER CHARACTERISTICS

Technology	0.18-μm CMOS
Filter Order/type	4^{th} /Chebyshev II
Power supply	2 V
Power consumption	3mW
DC gain	-1 dB
-3dB cutoff frequency	2.75 MHz
HD3(350mVpp@1MHz)	-46.3 dB
In-band IM3(-16dBm f1=1.75MHz,f2=2.25MHz)	-40 dB
In-band IIP3 (f1=1.75MHz,f2=2.25MHz)	+5 dBm
Input Referred Noise	70 μV_{rms}

V. CONCLUSION

With two feedforward capacitors, the proposed source-follower-based bi-quad cells are capable to synthesize useful complex zeros with a single branch fully differential structure for designing continuous time zero-pole type filters. A 4^{th}-order Chebychev II low-pass filter prototype using a cascade of two proposed cells has been fabricated in a 0.18-μm CMOS technology. The expected zero-pole characteristics of this filter have been confirmed experimentally. The power consumption is 3 mW and the achieved in-band IIP3 is 5 dBm under a 2-V supply.

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