A 12b 180MS/s 0.068mm^2 Pipelined-SAR ADC with Merged-residue DAC for Noise Reduction

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***Abstract*—This paper presents a 12b 180 MS/s partial-interleaving Pipelined-SAR analog-to-digital converter (ADC). The 1st-stage is implemented with a 2b/cycle SAR ADC for high speed, where we propose a merged-residue-DAC technique to improve the noise performance. The capacitor pre-charging in conventional 2b/cycle operation wastes settling time and switching energy, while with this design approach the switching procedure is optimized to avoid the pre-charging for tri-level reference generation. The prototype ADC fabricated in 65nm CMOS achieves a SNDR of 63.8dB @DC input with 6mW power dissipation from a 1.2V supply, leading to a FoM @DC of 26.3 fJ/conv.-step.**

I. Introduction

The performance of time-interleaving (TI)-ADCs [1][2] is limited by the offset, gain and timing mismatches among the channels. Though the first two characteristics can be easily measured and corrected in the digital domain, the clock skews are more difficult to be compensated [3]. These can be suppressed by timing calibrations [2][4] or avoided by ADC's architecture optimization [5] with an achievable accuracy around 9b. The partial-interleaving (PI) architecture reported in [5] avoids the timing mismatch by using a full-speed 2b/cycle SAR ADC for the front-end sampling and coarse conversion, while interleaving the residue multiplying digital-to-analog converters (MDACs) at the back-end. However, this architecture degrades the signal-to-noise ratio (SNR), as the kT/C noise is ultimately determined by the capacitance that is utilized in the amplification phase of the MDAC, which occupies only 25% of the total input capacitance [5]. On the other hand, if more bits can be resolved in the 1st-stage leading to relatively smaller output swing for the amplifier, it will relax the gain linearity requirement. But, the time assigned to the coarse conversion at the 1st stage is very limited, as the input capacitance is set by kT/C noise and matching requirements for full resolution, and DAC settling dominates the conversion speed. The multi-bit/cycle SA conversion can be adopted to break the speed bottleneck in the coarse stage. Plus, prior arts all required pre-charging to generate the corresponding reference levels before bit decisions [6][7]. Especially, when the leading bits are pre-charged, the current-induced reference ripples affect the fine conversion performed at the 2nd-stage. The interference via the reference source between two stages finally leads to signal-dependent errors that are difficult to be corrected.

This paper presents a 12-bit 180 MS/s PI Pipelined-SAR ADC to address the aforementioned issues. A merged-residue-DAC for a 2b/cycle operation is proposed that reduces the thermal noise impact with less design overhead. This approach keeps the total input capacitance small to fulfill the kT/C requirement only. Moreover, a pre-charging free switching method for 2b/cycle SAR conversion is adopt. When compared to conventional switching it achieves 68% and 38% average switching energy and reference ripple reductions, respectively. The Pipelined-SAR ADC prototype with the proposed techniques is fabricated in 65nm CMOS. Measurement results show an SNDR of 60.9 dB at Nyquist input, which corresponds to a FoM of 36.7 fJ/conv.-step. The ADC core occupies 0.068 mm^2 of die area including all the calibration circuitries.

II. ADC Architecture

Fig. 1 shows the overall PI Pipelined-SAR ADC architecture and its control timing diagram. The 1st-stage is built with a 7b (1b + 3×2b/cycle) SAR ADC operating at a full clock rate of 180 MS/s. By adopting an interpolation technique [8], the

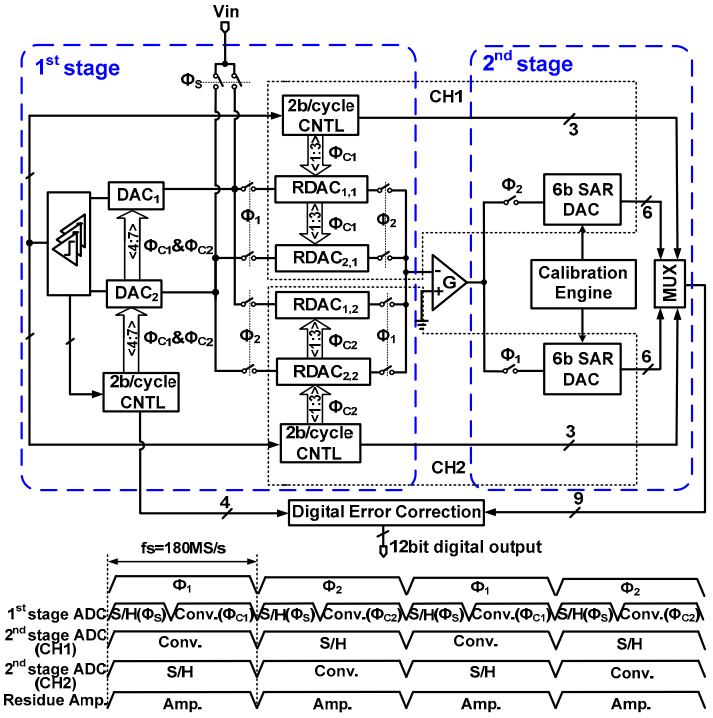

Fig. 1. PI Pipelined-SAR ADC architecture and timing diagram.

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2b/cycle SAR operation is implemented with only two capacitive DACs. Each DAC is composed of a common DAC (DAC_1 & DAC_2) and a ping-pong residue DAC ($RDAC_{1,1}$ & $RDAC_{2,1}$ / $RDAC_{1,2}$ & $RDAC_{2,2}$). One amplifier is shared by the ping-pong RDACs for residue amplification. The 2nd-stage is built with a 2×TI 6b SAR ADC, and each one operates at 90 MS/s. The two stages have one bit overlapping for digital error correction (DEC). The offset [9] and gain mismatches are all calibrated on-chip.

III. Merged-Residue-DAC Operation

For a 12b 180 MS/s 2×TI ADC design, the time skew needs to be suppressed to < 500 fs. To avoid the time skew the PI operation [5] is adopted in this design and Fig. 2 details the 1st stage operation. The 7b DAC is assigned as a segmented thermometer-code array to simplify the decoding logic. The capacitance ratio between the DAC_1 and the $RDAC_{1,1}$ is 1:3. When the sampling phase of Channel 1 is enabled (Φ_{S1}=1), the input signal is simultaneously sampled onto the top-plates of DAC_1 and DAC_2 associated with one pair of ping-pong RDAC, e.g. $RDAC_{1,1}$ and $RDAC_{2,1}$. Once the sampling is completed, the sampling switches SW_{S1} and SW_{S2} are turned off, thus separating the total units into two equivalent portions (upper and lower) for 2b/cycle SA operation. The TI switches $SW_{1,1}$ and $SW_{2,1}$ are kept on until the conversion of Channel 1 (Φ_{C1}) finishes. During the residue amplification phase (Φ_1=0 & Φ_2=1), the DAC_1 and the DAC_2 are disconnected from their previous TI counterparts, and connected to another pair $RDAC_{1,2}$ & $RDAC_{2,2}$ for the next sampling. Meanwhile the $RDAC_{1,1}$ and $RDAC_{2,1}$ are re-merged together and connected to the amplifier input for residue amplification.

Fig. 3 illustrates the 1st-stage DAC operation with thermal noise performance in each phase, for simplicity only one pair of TI RDAC is shown. In the sampling phase, two pairs of DACs (DAC_1 and $RDAC_{1,1}$, DAC_2 and $RDAC_{2,1}$) are connected together to sample the input, resulting in the total input capacitance C_{in} of 256C that satisfies the 12b kT/C noise. In the coarse 7b conversion, the comparison accuracy is relaxed to 8b due to the DEC. Thus, the capacitance in each pair is sufficient for the required noise. In the amplification phase, as the residue needs to be accurate to the overall ADC precision, two RDACs are disconnected from their corresponding DACs and re-merged together for amplification, leading to a total amplification capacitance C_{amp} as large as 192C. Compared to our previous design [5] with same resolution, C_{in} in this design

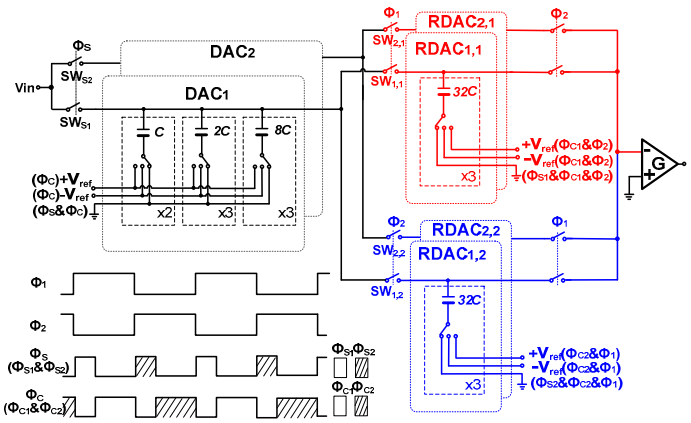

Fig. 2. Implementation of the 1st-stage DAC (single-ended).

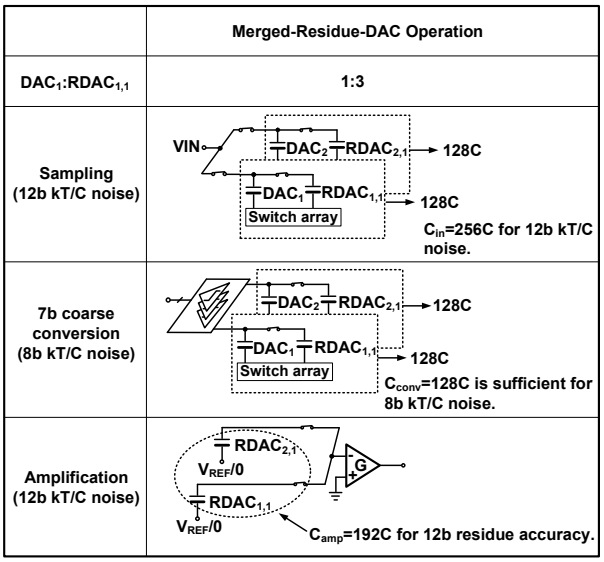

Fig. 3. The 1st-stage DAC operation with the noise performance in different phases.

is reduced by 2, while the C_{amp}/C_{in} is increased from 25% to 75%. The 2b/cycle conversion usually achieves higher conversion speed with the penalty of doubling the C_{in}, while the merged-residue-DAC operation allows a 2b/cycle conversion with the C_{in} downsized to the kT/C limitation, and meanwhile enabling a PI scheme with better noise performance. With C_{in} of 1.4 pF in this design, the total input-referred noise is 133μV-rms according to the simulation results, which is sufficient for 12b accuracy.

IV. Pre-Charging Free Switching Method

In a conventional 2-bit/cycle SAR ADC, the pre-charging operation is necessary to generate the tri-reference levels needed for comparison, while the proposed switching avoids it. Thus, it can trade extra idle time to resolve more bits. Fig. 4 illustrates a 3-bit design example using conventional and proposed switching methods, where the 1b+2b/cycle and worst case for energy efficiency is described here. When sampling phase (Φ_S) is enabled, the input is sampled onto both top-plates of the DACs (DAC_A and DAC_B), while the bottom-plates are all reset to Gnd. The MSB is determined by simply comparing the input polarity. If V_{IN}<0, two "2C" will be switched to V_{REF}. Then, the MSB transition is completed. For the coming 2b comparisons, V_{IN} should be compared with three thresholds, i.e. -1/4V_{REF}, -1/2V_{REF} and -3/4V_{REF}. Conventionally, the pre-charging phase is required to discharge and charge another "2C" in DAC_A and DAC_B, respectively. As V_{IN} is within the range from -1/2V_{REF} to -1/4V_{REF}, accordingly, after the 2b transitions the final residue will be V_{IN}+3/8V_{REF}.

In the proposed switching, the MSB transition and pre-charging phase are merged together, where in DAC_A only one "2C" is charged up that generates the same residue as the conventional one at the DAC_A output. For the coming 2b transition, to reduce the reference ripple only one "C" in the DAC_B is discharged to -V_{REF} and "2C" is discharged back to the common-mode level rather than -V_{REF}, as the common-mode is insensitive to its ripples in differential operation. The total switching energy drawn from references is composed of two parts. The first part comes from the bit transition where the corresponding units are switched to V_{REF} or -V_{REF}. Obviously,

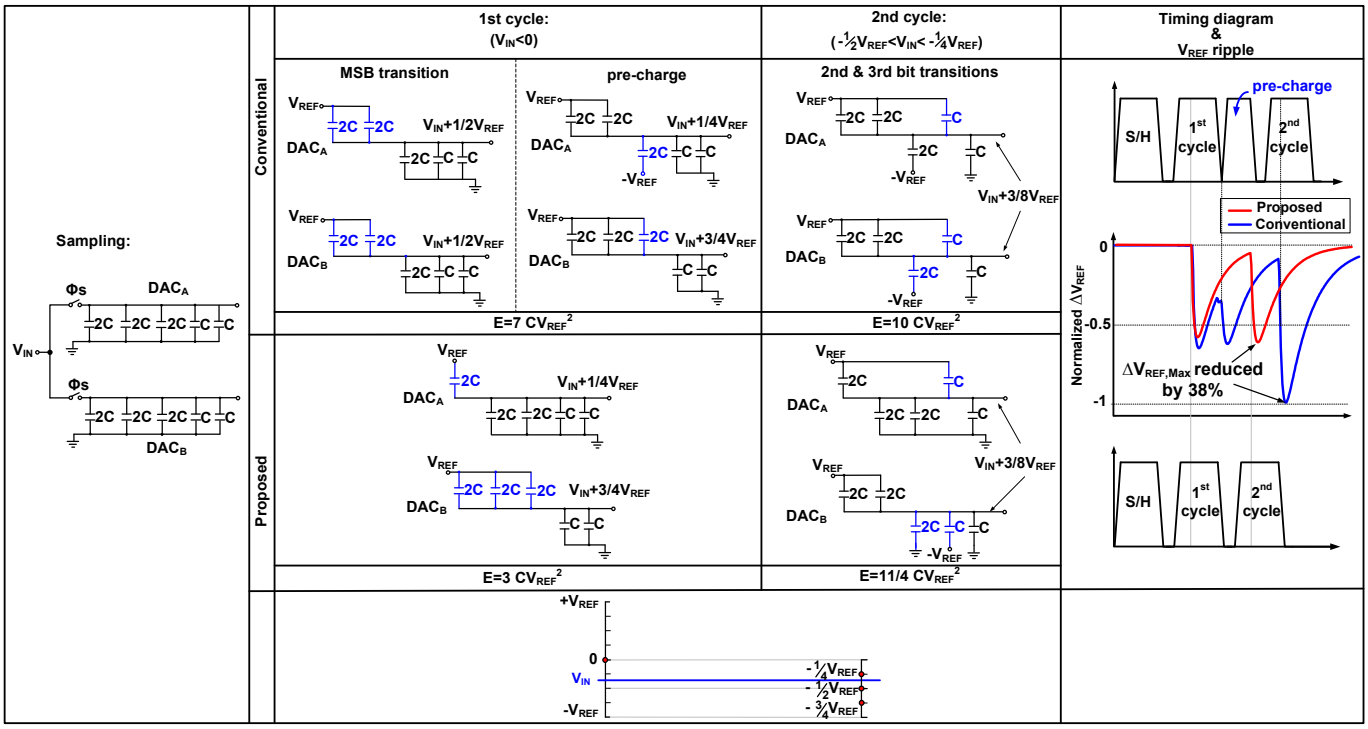

Fig. 4. Comparison between the conventional and proposed switching operations (single-ended).

in the conventional case, there are more units involved in residue generation than in the proposed circuit. The second part comes from the units previously kept connected to reference voltages, where the energy is consumed to drive the change in the DAC output. As shown in Fig. 4 for the switching during the 2nd cycle, there are a total of 10 units previously connected to reference voltages in the conventional case, while in the proposed case there are only 6 units. Consequently, it achieves 73% switching energy reduction. Also, since less number of units is switched, the reference ripple can be reduced by 38%. Avoiding the pre-charging phase spares more time for the 1st stage conversion, which can be used to determine one more bit. Therefore, in this design a 7-bit with 1b + 3×2b/cycle SAR is implemented. Fig. 5 shows a behavioral simulation that compares the switching energy based on the conventional and proposed approaches for a 7-bit SAR ADC. The average switching energy of the conventional method is 152 CV_{REF}^2 whereas the proposed method requires only 48.5 CV_{REF}^2, thus achieving a 68% reduction. The proposed switching optimizes the transitions for a 2b/cycle operation that obtains less charge transfer implying the reduction of both switching energy and reference ripple.

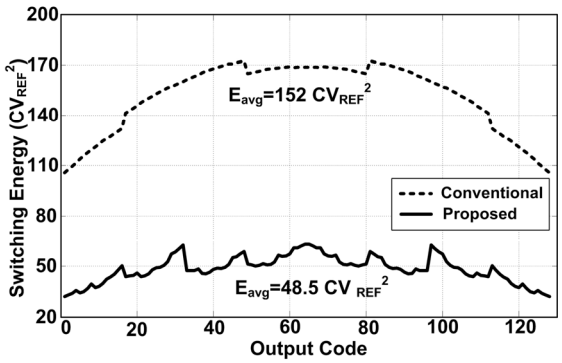

Fig. 5. The energy versus output code for different switching methods.

V. Experimental Results

The prototype ADC was fabricated in a 1P7M 65nm CMOS. The die photo shown in Fig. 6 indicates that the ADC core occupies an active area of 0.068 mm^2 including all calibration circuits for offset and gain mismatches. Fig. 7 shows the measured SNDR of 5 chips @ near DC input, whose average SNDR is 63.24 dB. Fig. 8 shows the measured FFTs after the calibration @ ~DC and Nyquist input frequencies, respectively. The SNDR and SFDR with low frequency input are 63.8 dB and 76.3 dB, respectively. The SNDR drops by nearly 3 dB at Nyquist input, which is mainly limited by the clock jitter. The design also shows the good immunity to the timing mismatch, where the interleaving spur is maintained at -77 dB @ Nyquist input. The measured dynamic performances are plotted in Fig. 9. The SNDR remains > 60 dB as the input frequency goes up to 100 MHz. The ADC achieves a peak SNDR of 64.5 dB @ 10 MHz input and fs=120 MS/s.

The total power consumption of the ADC including the calibration circuit is 6 mW, where 2.8 mW is from the analog part and 3.2 mW from the digital. The FoM @DC and @Nyquist at 180 MS/s are 26.3 fJ/conv.-step and 36.7 fJ/conv.-step, respectively. Table I summarizes the performance of this work, and when comparing it with the state-of-the-art high-speed pipeline and Pipelined-SAR ADCs, this design achieves competitive conversion accuracy and FoM with small area.

VI. Conclusions

A 12-bit 180 MS/s Pipelined-SAR ADC has been presented. The merged-residue-DAC operation enables a PI scheme without the degradation of noise performance. The proposed 2b/cycle switching approach avoids the pre-charging operation

and leads to better energy efficiency and lower reference noise. The prototype achieves 60.9 dB SNDR and 67.17 dB SFDR at the Nyquist, consumes 6 mW and occupies 0.068 mm^2 area in 65nm CMOS.

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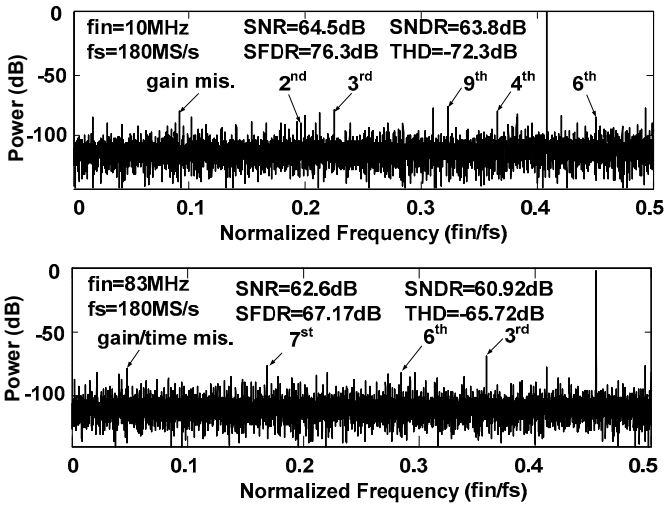


Fig. 8. Measured FFT of the digital output decimated by 25.

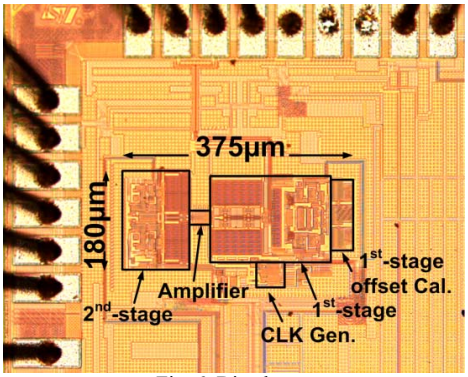


Fig. 6. Die photo.

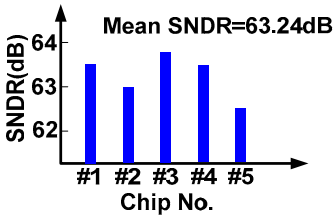
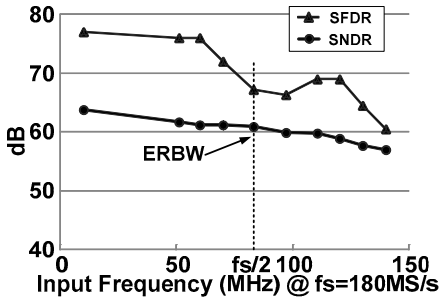
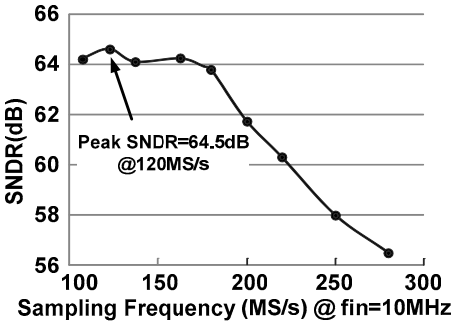


Fig. 7. Measured SNDR of 5 chips @ fin=10MHz, fs=180MS/s.



(a)



(b)

Fig. 9. Measured dynamic performances. (a) SNDR/SFDR vs. input. (b) SNDR vs. clock frequency.

TABLE I: Performance Summary and Comparison

	VLSI'14 B. Verbreggen	VLSI'14 Y. Zhou	VLSI'13 N. Dolev	VLSI'14 C-Y Lin	This Work
Architecture	Pipeline-SAR	Pipeline-SAR	Pipeline	Pipeline-SAR	Pipeline-SAR
Technology (nm)	28	40	65	65	65
Resolution (bit)	14	12	12	12	12
Sampling Rate (MS/s)	200	160	200	210	180
Supply Voltage (V)	0.9	1.1	1.2	1	1.2
Power (mW)	2.3	4.96	11.5	5.3	6
SNDR@Nyq.(dB)	65	65.3	57.6	60.1	60.92
SNDR@DC(dB)	70	66.5	65	63.48	63.8
FoM@Nyq. (fJ/conv.-step)	8.87	20.7	92.8	30.3	36.7
FoM@DC (fJ/conv.-step)	4.44	17.7	39.6	20.7	26.3
Area (mm^2)	0.1	0.042	0.26	0.48	0.068 (gain & offset Cal. logic included)
On-chip Cal.	No	No	No	No	Yes