Seven-bit 700-MS/s Four-Way Time-Interleaved SAR ADC With Partial V_{cm}-Based Switching

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***Abstract*— This brief presents a 7-bit 700-MS/s four-way time-interleaved successive approximation register (SAR) analog-to-digital converter (ADC). A partial V_{cm}-based switching method is proposed that requires less digital overhead from the SAR controller and achieves better conversion accuracy. Compared with switchback switching, the proposed method can further reduce the common mode variation by 50%. In addition, the impacts of such a reduction on the comparator offset, noise, and input parasitic are theoretically analyzed and verified by simulation. The prototype fabricated in a 65-nm CMOS technology occupies an active area of 0.025 mm^2. The measurement results at the 700 MS/s sampling rate show that the ADC achieves signal-to-noise-and-distortion ratio of 40 dB at Nyquist input and consumes 2.72 mW from a 1.2 V supply, which results in a Walden FoM of 48 fJ/conversion step.**

***Index Terms*— Common mode variation, partial V_{cm}-based switching, time-interleaved successive approximation register analog-to-digital converter (TI SAR ADC).**

I. Introduction

High-speed (>500 MS/s sampling rate) and low-to-medium-resolution (5- to 7-bit) ADCs are widely utilized in ultrawide band communication systems [1]. The successive approximation register (SAR) ADC is a power efficient architecture due to its fully dynamic operation and simple structure, as well as its benefits over technology scaling. With the development of modern nanometer CMOS technologies and advanced circuit solutions, the SAR ADC can achieve high speed [1]–[3] and becomes a competitive alternative for such applications.

The switching approach for the capacitive digital-to-analog converter (DAC) is adopted due to its conversion linearity, speed, and energy efficiency. Several switching techniques have been proposed to improve the power efficiency of the capacitive DAC [4]–[10]. The SAR ADCs for low-speed applications (<1 MS/s), within sensor networks and implantable biomedical devices, can benefit from the advanced switching significantly, since its switching energy occupies a large part of the power consumption [4]. However, if the SAR ADC is designed for high speed, its power is dominated by the digital part, i.e., the SAR controller. Typically, the switching energy occupies less than 15% of the total ADC power dissipation [1], [3]. Therefore, the methods that mainly reduce the switching energy are not very effective for high-speed SARs. The monotonic and switchback switching methods [5], [6] simplify the control logic for SAR conversion and achieve good energy efficiency for high speed, whereas they both suffer from common mode variation during the bit cycling. The common mode variation in the comparator is much more critical as it induces the dynamic offset, noise, and the input parasitic variation, which significantly affects the speed and accuracy of the comparisons. The switchback switching method [6] reduces the common mode variation by 50% compared with the monotonic switching approach [5]. However, as the switchback operation is pure single ended, it still leads to a larger common-mode variation in comparison with the conventional switching. An improved capacitor splitting method is proposed in [7] to alleviate the common mode variation issue. Only the least significant bit (LSB) transition induces a small common mode variation with two reference voltages. However, the split DAC makes the routing and the control logic of the switches being more complex and the quantity of switches need to be doubled.

This brief presents a 7-bit 700-MS/s four-way time-interleaved SAR ADC (TI SAR ADC), achieving a signal-to-noise-and-distortion ratio (SNDR) of 40 dB at Nyquist input with a 2.72-mW power dissipation. A partial V_{cm}-based switching method is proposed to improve conversion linearity, which causes less complexity for the SAR logic implementation and consumes less power on logic than the pure V_{cm}-based switching method [8], [9]. In contrast to the switchback switching, the common mode variation can be further reduced by another 50%. The conversion nonidealities due to common mode variation including dynamic offset, noise, and voltage-dependent parasitic is theoretically analyzed and validated by simulation results. Finally, the measurements of the various ADC static and dynamic performances are also provided.

II. ADC Architecture

The time-interleaved (TI) scheme is a common approach to enhancing the conversion speed of ADCs [1] and the TI SAR ADC can achieve an excellent power efficiency with a sampling rate range between 500 and 900 MS/s [11]. The overall ADC architecture is shown in Fig. 1(a), which consists of 7-bit four-way TI ADCs operating at 175 MS/s for an aggregate 700-MS/s sampling rate.

The sub-ADC is built with a conventional SAR architecture, which contains a capacitive DAC, a dynamic comparator, and an SAR controller. Matching of capacitive DAC is limited by both process variation and systematic layout mismatches, and it limits the overall linearity of the converter. The custom-designed metal–oxide–metal capacitor is used as unit capacitance in this brief. The value of unit capacitance is 5 fF. Its variation σ_C is within 0.1% (obtained in the data sheet with a similar capacitor structure), which well meets

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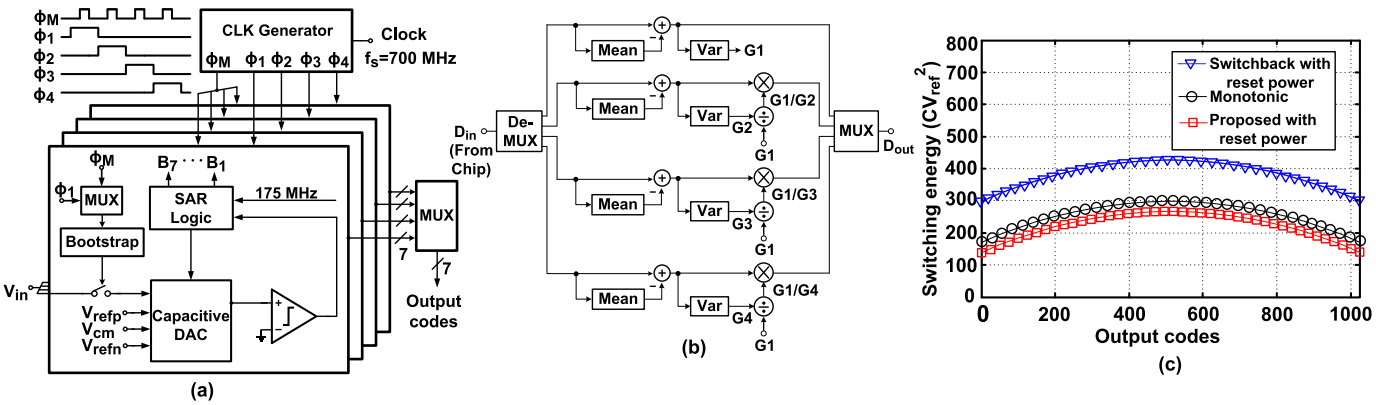

Fig. 1. (a) Overall ADC architecture. (b) Offset/gain mismatches calibration. (c) Switching energy versus output code of a 10-b SAR, including the reset power during sampling.

the requirement for the 7-bit resolution ($\sigma_C < 4.4\%$ for 7-bit). The binary-weighted capacitor array with the attenuation capacitor structure is adopted [9]. Compared with the conventional binary-weighted capacitor array, the number of unit capacitors is reduced from 64 to 19, and with an additional bridge capacitor C_A, the capacitor array can be very compact, which simplifies the routing. The four channels are identical copies.

The TI scheme suffers mismatches from offset, gain, and timing skew. The offset and gain mismatches are mainly caused by the comparator offset and the parasitic capacitance of the capacitor array. The time skew originates from the timing mismatch of sampling instance. The offset and gain mismatches can be calibrated off-chip in the digital domain by averaging and variation functions [12], as illustrated in Fig. 1(b). First, the digital codes from the chip are divided into four channels by a demultiplexer (De-MUX), and then the codes are averaged by mean function in each channel. The information of offset voltage is acquired. The codes subtract their mean values and then they are combined into one stream by a multiplexer (MUX). Eventually, the offset mismatch is removed in the digital domain with code subtraction. The gain error information is acquired by a mean-square-deviation function, G1–G4 are the gain factors of channels 1–4, and then the factors of channels 2–4 are normalized to channel 1. The codes multiply these factors and they are combined into one stream by the MUX. Then, the gain mismatch is removed in digital domain. As this design uses the top-plate sampling, the gain mismatches due to mismatch of routing and top-plate parasitics are suppressed by symmetrical and compact routing of the DAC for the 7-bit resolution and no gain calibration is required. It is verified with measurement at dc input. Before calibration, the gain spurs are below -62 dB and the SNDR is 41 dB. After calibration, the gain spurs are below -67 dB and the SNDR is 41.1 dB, which implies the gain mismatch is not the main limitation of the ADC. The gain mismatch calibration is not required and can be disabled in this design. After the offset/gain calibration, the time skew becomes the main design limitation in TI ADCs. In this design, the sampling instances of the TI channel is synchronized with the master clock ϕ_M, which is selectively applied to four TI channels via an MUX controlled by the clock signals $\phi 1$ to $\phi 4$ [13]. The simulated variation of time skew $\sigma_t = 1.7$ ps. Such a solution can effectively suppress the interleaving spurs below -53 dB. The routing of the sampling clocks is also symmetrical between channels.

III. Proposed Switching Scheme

A. Review of Switchback Switching

The monotonic and switchback approaches optimize both energy efficiency from switching and control logic compared with the conventional scheme. Since their operation is single ended, where one of the differential DACs is charged or discharged in each bit cycling, the energy saving in the controller is more significant. However, they both suffer from conversion nonlinearities induced by the common mode variation during each bit comparison.

A 4-bit example performing the switchback approach is demonstrated in Fig. 2(a). As the operation of most significant bit (MSB) is single ended with only one of the differential DACs discharged, the common mode voltage drops by $V_{\text{ref}}/4$, as shown in Fig. 2(b1). The transitions of the two leading bits result in the larger common mode variation, which can be released by the proposed partial V_{cm}-based switching.

B. Proposed Partial V_{cm}-Based Switching Technique

A partial Vcm-based switching approach is proposed that not only maintains good energy efficiency from both switching and logic controllers but also improves the common mode variation compared with the switchback approach. The switching scheme is shown in Fig. 2(a). During the sampling phase, the input signal is sampled onto the top plate of the capacitive DAC, where the bottom plate of the two leading bits and the rest of the bits are connected to V_{cm} and V_{ref}, respectively. In the conversion phase, the MSB decision is made directly by comparing the difference between the differential inputs. For example, if $V_{\text{op}} > V_{\text{on}}$, the MSB capacitor in DAC$_p$ and DAC$_n$ is switched from V_{cm} to Gnd and V_{ref}, respectively. The operation repeats for the MSB/2 transition. As the operation of the two leading bits is differential, its common mode remains constant. For the rest of the bits cycling, the corresponding bit in one of the DAC will be discharged to Gnd. For an n-bit ADC, the operation repeats $n-3$ times until the last bit is determined. Although the operation of the LSBs are single-ended, which cause common mode variation, the amount is much smaller than the switchback approach. As shown in Fig. 2(b2) the maximum variation is $V_{\text{ref}}/8$ that is 50% lower than the switchback method. Furthermore, as only the two leading bits are involved in V_{cm}-based switching, the design complexity and digital overhead from the controller is not significant.

Unlike our previous work [8] (V_{cm}-based switching) the proposed partial V_{cm}-based switching consumes power during the sampling phase. While for conversion the DAC operates differentially, it does not draw the power from V_{cm} and its ripple will not affect the conversion accuracy. For an n-bit SAR ADC, the average switching energy of the proposed method can be derived as

$$E_{\text{Avg,Par-Vcm}} = \sum_{i=1}^{2} (2^{n-2-2i})(2^i - 1)\text{CV}_{\text{ref}}^2 + \sum_{i=3}^{n-1} (2^{n-2-i})\text{CV}_{\text{ref}}^2 \quad (1)$$

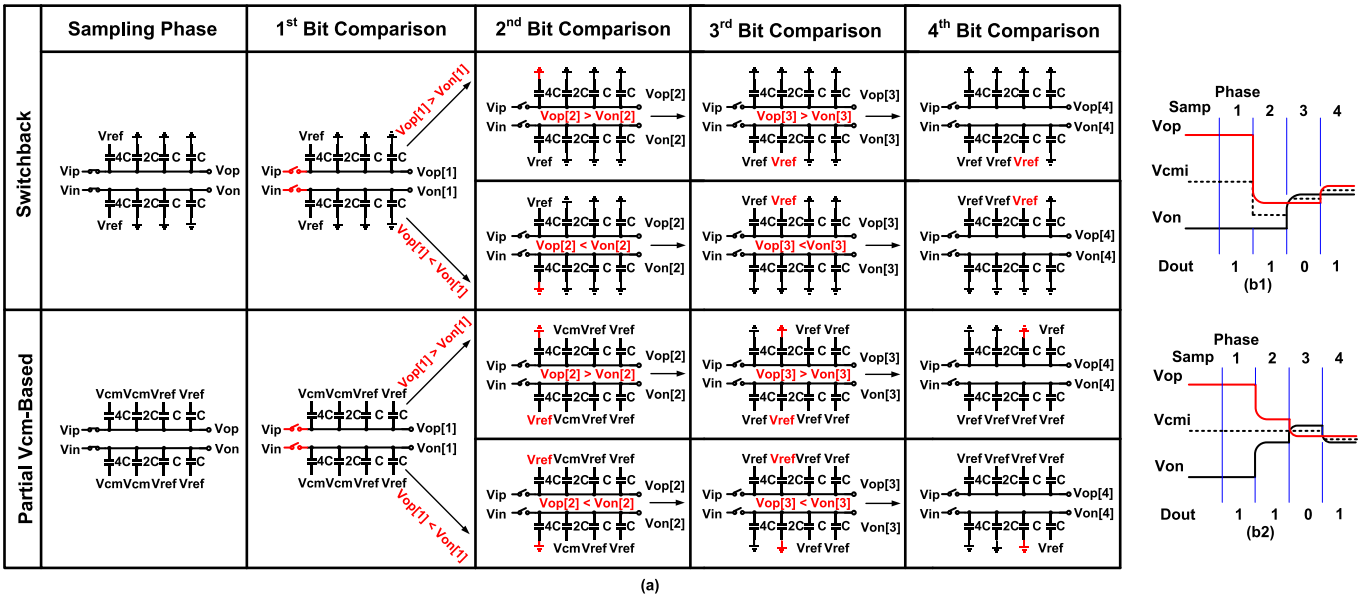

Fig. 2. (a) 4-b example of switchback and partial $V_{\rm cm}$-based switching procedures. (b1) Comparator input common mode variation for switchback switching. (b2) Comparator input common mode variation for the proposed switching.

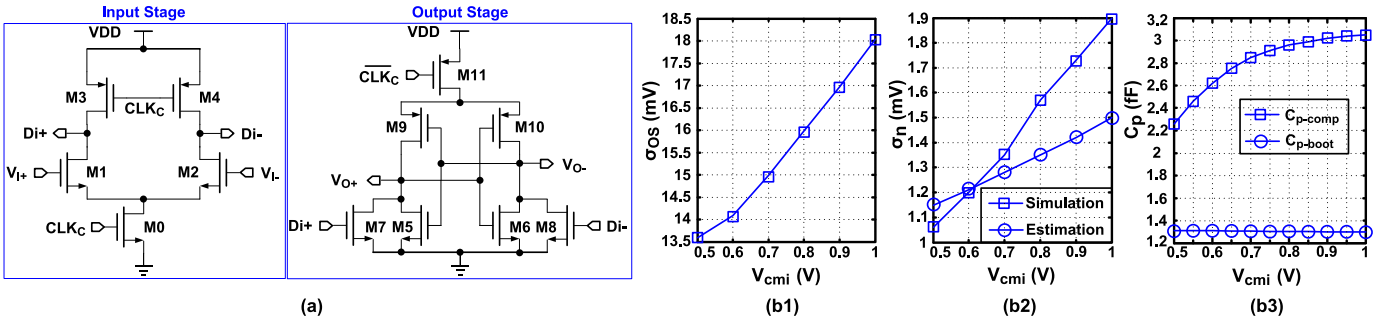

Fig. 3. (a) Schematic of double tail dynamic comparator. (b1) Simulated comparator offset versus input common mode voltage. (b2) Simulated comparator noise versus input common mode voltage. (b3) Parasitic capacitance $C_{p\text{-comp}}$ and $C_{p\text{-boot}}$ versus input common mode voltage.

where C is the unit capacitance and $V_{\rm ref}$ is the reference voltage. For a 10-bit case including the reset energy from the sampling, the total energies consumed by monotonic and switchback switching are 255.5 and 383 $CV^2_{\rm ref}$ [6], respectively, while the proposed method consumes 223.5 $CV^2_{\rm ref}$, which includes the energy (48 $CV^2_{\rm ref}$) from the $V_{\rm cm}$ input during sampling. Fig. 1(c) shows a comparison of the switching energy obtained from the equation for the three methods.

C. Comparator With Common Mode Variation

The common mode variation is a critical problem that degrades the conversion accuracy of the SAR ADC, as the operating point of the comparator is affected, leading to dynamic offset, voltage-dependent parasitic, and input-referred noise variation. The double tail dynamic comparator [14] is used in this design, whose schematic is shown in Fig. 3(a).

In order to suppress the input-referred offset and noise of the output latch stage, a large voltage gain is required at the comparator's input stage. As the gain of the dynamic amplifier is defined by $g_m \times T_a/C$ (g_m is the transconductance of the input transistors, T_a is the time for amplification, and C is the capacitance load), it is important to maintain the input transistors in the saturation region for a specific time of amplification (T_a) [15]. The voltage at node D_i drops with the discharging rate defined by $I_{\rm tail}/(2C)$ in the amplification phase, where $I_{\rm tail}$ is the tail current of the first stage. The amplification

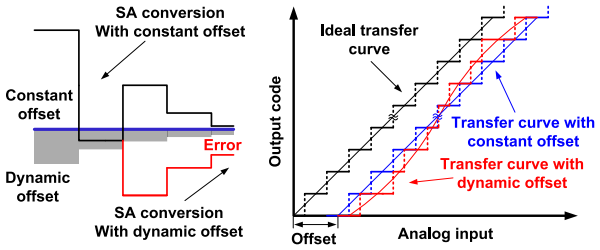

Fig. 4. Impact of constant offset and dynamic offset.

time is inversely proportional to the discharging rate, and the common mode voltage has an impact on the time for amplification. When the input common mode is higher, the discharging rate is larger, and this leads to a shorter value of T_a, so the preamplifier gain drops with input common mode voltage.

Relevant SPICE level simulations are performed to verify the above assumptions. The aspect ratio of the comparator's input pair is 3 μm/0.06 μm. The supply voltage is 1.2 V and the clock frequency is 1.5 GHz. The simulation result reveals that the voltage gain depends strongly on the input common mode voltage $V_{\rm cmi}$. For partial $V_{\rm cm}$-based switching, the gain is maintained above 15 when $V_{\rm cmi}$ increases from 0.6 to 0.725 V. The input-referred offset and noise of the second stage can be significantly reduced. On this account, the

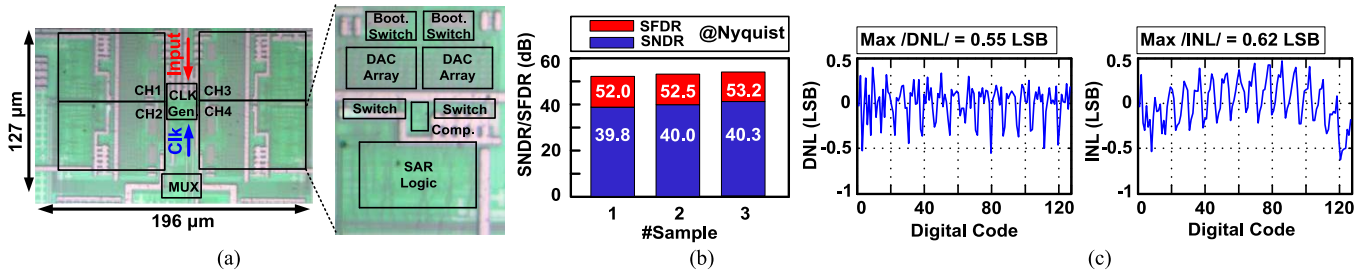

Fig. 5. (a) Die micrograph. (b) Measured SNDR and SFDR from three samples at Nyquist input and $f_s = 700$ MHz. (c) Measured DNL/INL.

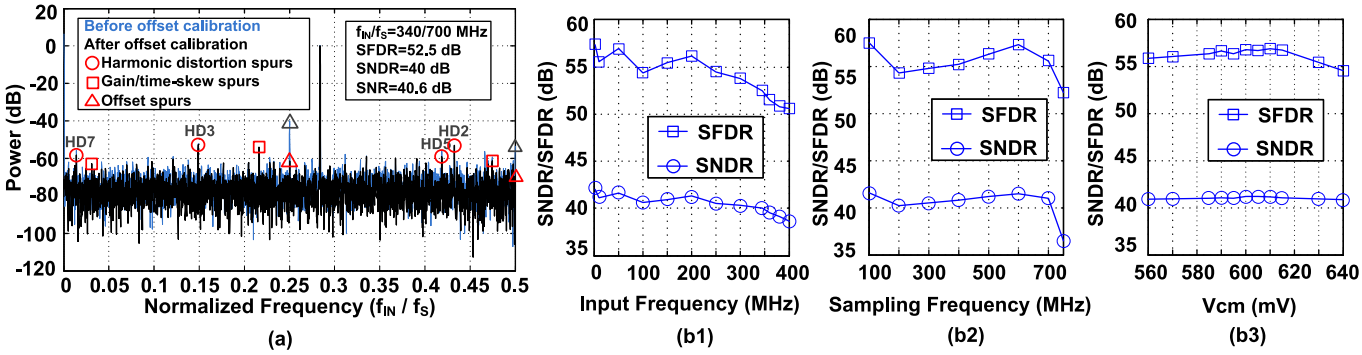

Fig. 6. (a) Measured 8192-point power spectrum at near-Nyquist input with $f_s = 700$ MHz (decimated by 125). Measured dynamic performance SNDR and SFDR versus (b1) f_{IN} at $f_s = 700$ MHz, (b2) f_s at $f_{\text{IN}} = 10$ MHz, and (b3) V_{cm} reference voltage at $f_{\text{IN}} = 10$ MHz and $f_s = 700$ MHz.

offset and noise contributions of the first stage become dominant [15].

1) Comparator Offset: The offset voltage of the input transistor is affected by device mismatches and bias conditions [5]. The common mode voltage determines the overdrive voltage of the input pair, and its variation during each bit SAR conversion will induce a dynamic offset. The dynamic comparator shown in Fig. 3(a) is used to perform the SPICE level simulation. The simulation condition is the same as mentioned before. Fig. 3(b1) shows the relation between the common mode voltage and offset voltage at one sigma obtained from 100 times Monte Carlo simulations. The offset voltage of the comparator increases when V_{cmi} increases. For switchback and partial V_{cm}-based switching, the maximum dynamic offsets induced by common mode voltage variation are around 2 and 1 mV, respectively. The impact of the offset voltage on the ADC conversion is illustrated in Fig. 4. For a single-channel ADC, the constant offset voltage only causes a dc voltage shift and does not influence the accuracy of the ADC conversion. For TI SAR ADC, the offset of each channel induces the offset mismatch. The dynamic offset influences the decision of the comparator during the conversion phase in both single-channel and TI SAR ADCs, and this causes the conversion error and nonlinearity. With the partial V_{cm}-based switching, the simulated dynamic offset of the comparator is about 1 mV, which is far less than 1/2 LSB of the ADC with the 7-bit resolution. The influence of dynamic offset is reduced greatly.

2) Comparator Noise: The input-referred noise of the differential input pair σ_n can be estimated by (2) and noise bandwidth NBW can be expressed as (3) [16]

$$\sigma_n \approx \sqrt{8 \cdot k \cdot T \cdot \frac{\gamma}{g_m} \cdot \text{NBW}} \tag{2}$$

$$\text{NBW} = \frac{1}{2 \cdot T_{\text{int}}} \tag{3}$$

where g_m is the transconductance of the input transistors. The factor γ could be as high as 2.5 for a 65-nm CMOS technology. T_{int} is the integration time. The common mode voltage has an impact on g_m and NBW. Fig. 3(b2) shows the simulated and estimated values of the comparator input-referred noise versus the input common mode voltage V_{cmi}. When common mode voltage is low, the simulation results are in good agreement with the estimated values. When common mode voltage is high, there is a slight difference between them. This is because the gain of the preamplifier decreases as V_{cmi} increases. Although the input-referred noise of the first stage is also dominant, the influence of the second stage becomes nonnegligible. For partial V_{cm}-based switching, σ_n increases from 1.2 mV at $V_{\text{cmi}} = 0.6$ V to 1.42 mV at $V_{\text{cmi}} = 0.725$ V, the noise level fluctuation is small, and it will not degrade the performance of the ADC.

3) Comparator Parasitics: It is important to note that the parasitic capacitance C_p exists at the comparator input terminals. It consists of signal-independent parasitics $C_{p\text{-cap}}$, associated with parasitics of the comparator's differential pair $C_{p\text{-comp}}$ and the bootstrapped sampling switch $C_{p\text{-boot}}$. The values of $C_{p\text{-comp}}$ and $C_{p\text{-boot}}$ versus common mode voltage V_{cmi} are plotted in Fig. 3(b3), and the aspect ratios of the comparator's input pair and bootstrapped sampling switch are 3 μm/0.06 μm and 6 μm/0.06 μm, respectively. The variation of $C_{p\text{-boot}}$ is small and nearly constant. This is because the bootstrapped sampling switch is OFF during the conversion phase and then less affected by the common mode variation. $C_{p\text{-comp}}$ is signal dependent and increases as V_{cmi} increases. With the proposed switching method, $C_{p\text{-comp}}$ has only a peak variation of 0.22 fF. For the switchback, V_{cmi} varies from 0.5 to 0.75 V, and $C_{p\text{-comp}}$ has a peak variation of 0.7 fF. The variation of C_p will affect the linearity of the ADC and introduce harmonics [6]. In order to overcome the influence of parasitic variation, the size of the sampling capacitance with switchback is threefold larger than that of the proposed method. A constant current biased preamplifier is also utilized in [6] to keep the overdrive voltage of the input pair near a constant value, leading to more static power. Instead of preamplifier utilized in [6],

TABLE I
COMPARISON WITH STATE-OF-THE-ART WORKS

Paper	ISSCC 14' M. Miyahara [17]	VLSI 12' Y. C. Lien [2]	JSCC 15' H. K. Hong [3]	This work
Architecture	Folding Flash	2b/cycle SAR	2b/cycle SAR	TI SAR
Techonology	40 nm	28 nm	45 nm	65 nm
Input cap.	300 fF (S/H)	150 fF	600 fF	160 fF
Resolution	7-bit	8-bit	7-bit	7-bit
f_s (MS/s)	2200	750	1000	700
Supply voltage (V)	1.1	1	1.25	1.2
DNL/INL(LSB)	0.6/1	0.6/0.57	0.4/0.5	0.55/0.62
SNDR (dB) @Nyquist	37.4	43.3	40.8	40
Power (mW)	27.4	4.5	7.2	2.72
FOM@Nyquist (fJ/Conv.-step)	205.7	50	80	48
Area (mm^2)	0.052	0.004	0.016	0.025

a dynamic preamplifier shown in Fig. 3(a) is adopted in this design. With the increase in ADC resolution, the size of the comparator input pair becomes larger, and the impact of common mode variation on parasitic variation becomes more serious.

IV. MEASUREMENT RESULTS

The prototype ADC was fabricated in a 1P9M 65-nm CMOS technology. Fig. 5(a) shows the micrograph of the ADC core whose total active area is 0.025 mm^2 (196 μm $\times$ 127 μm).

The input capacitance of the sub-ADC is 160 fF. The SNDR and spurious-free dynamic range (SFDR) of three measured samples at Nyquist input and $f_s = 700$ MHz are illustrated in Fig. 5(b). The SNDR and SFDR are 40 and 52.5 dB, respectively, in the mean performance sample. The sample NO.2 was selected to report the following results.

The measured static performance is shown in Fig. 5(c). The differential nonlinearity (DNL) and integral nonlinearity (INL) are $+0.39/-0.55$ LSBs and $+0.46/-0.62$ LSBs, respectively. Fig. 6(a) shows the measured FFT of the ADC at near-Nyquist input and the frequency of input signal is around 340 MHz, where the SNDR limited by the offset mismatches before calibration is 35.3 dB and improved to 40 dB after calibration. The clock jitter limits the SNR to around 40.6 dB. The third harmonic dominates the SFDR at 52.5 dB and the gain/skew spurs are below -53 dB. According to the measurement at dc input, the gain spurs are all below -62 dB, implying that the gain mismatch is not the main design limitation.

Fig. 6(b1) plots the measured SNDR and SFDR versus the input frequency at a sampling rate of 700 MS/s, where SNDR is kept near 40 dB from dc to Nyquist inputs. Fig. 6(b2) shows the measured dynamic performance versus the sampling frequency ata 10-MHz input. Fig. 6(b3) plots the measured SNDR and SFDR versus $V_{\rm cm}$ reference voltage.

The total power consumption is 2.72 mW, including a 0.56-mW analog power from track and hold (T/H), DAC, and comparators and a 2.16-mW digital power from the clock generator and the SAR logic. For the testing purpose, the three reference voltages are generated off-chip. The decoupling capacitors are added on-chip to reduce the impact of package bond wire *LC* resonance on reference settling time. According to measurement, the power dissipation of $V_{\rm cm}$ is only 55 μW, which is quite small. Therefore, the buffer of $V_{\rm cm}$ can be generated on-chip with small power dissipation. The achieved figure of merit is 48 fJ/conversion step at Nyquist. Table I compares the proposed ADC with other state-of-the-art ADCs [2], [3], [17]. This design obtains an excellent energy efficiency for high speed and medium resolution. The input capacitance mainly refers to the sampling capacitance.

V. CONCLUSION

A 7-bit 700-MS/s four-way TI SAR ADC has been presented. A partial $V_{\rm cm}$-based switching method is proposed to reduce the parasitic capacitance variation, the comparator dynamic offset, as well as the noise variation induced by common mode fluctuation. Compared with switchback switching, the proposed method can further reduce the common mode variation by 50%. The prototype occupies an active area of 0.025 mm^2 and achieves a 6.3 ENOB with a 2.72-mW power consumption.

REFERENCES

[1] P. J. A. Harpe, *et al.*, "A 0.47–1.6 mW 5-bit 0.5–1 GS/s time-interleaved SAR ADC for low-power UWB radios," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1594–1602, Jul. 2012.

[2] Y.-C. Lien, "A 4.5-mW 8-b 750-MS/s 2-b/step asynchronous subranged SAR ADC in 28-nm CMOS technology," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2012, pp. 88–89.

[3] H.-K. Hong *et al.*, "A decision-error-tolerant 45 nm CMOS 7 b 1 GS/s nonbinary 2 b/cycle SAR ADC," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 543–555, Feb. 2015.

[4] F. M. Yaul *et al.*, "A 10 b 0.6 nW SAR ADC with data-dependent energy savings using LSB-first successive approximation," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 198–199.

[5] C.-C. Liu, *et al.*, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010.

[6] G.-Y. Huang, *et al.*, "10-bit 30-MS/s SAR ADC using a switchback switching method," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 21, no. 3, pp. 584–588, Mar. 2013.

[7] V. Tripathi *et al.*, "An 8-bit 450-MS/s single-bit/cycle SAR ADC in 65-nm CMOS," in *Proc. IEEE ESSCIRC*, Sep. 2013, pp. 117–120.

[8] Y. Zhu *et al.*, "A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1111–1121, Jun. 2010.

[9] Y. Zhu *et al.*, "Split-SAR ADCs: Improved linearity with power and speed optimization," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 2, pp. 372–383, Feb. 2014.

[10] Z. Zhu *et al.*, "A 0.6-V 38-nW 9.4-ENOB 20-kS/s SAR ADC in 0.18-μm CMOS for medical implant devices," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 9, pp. 2167–2176, Sep. 2015.

[11] H.-K. Hong *et al.*, "An 8.6 ENOB 900 MS/s time-interleaved 2 b/cycle SAR ADC with a 1 b/cycle reconfiguration for resolution enhancement," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 470–471.

[12] Y.-C. Huang, *et al.*, "A 10-bit 400-MS/s 36-mW interleaved ADC," in *Proc. IEEE RFIT*, Nov./Dec. 2011, pp. 181–184.

[13] B. Verbruggen, *et al.*, "A 2.6 mW 6 bit 2.2 GS/s fully dynamic pipeline ADC in 40 nm digital CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 2080–2090, Oct. 2010.

[14] S. Babayan-Mashhadi *et al.*, "Analysis and design of a low-voltage low-power double-tail comparator," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 2, pp. 343–352, Feb. 2014.

[15] C.-H. Chan, *et al.*, "A reconfigurable low-noise dynamic comparator with offset calibration in 90 nm CMOS," in *Proc. IEEE A-SSCC*, Nov. 2011, pp. 233–236.

[16] M. van Elzakker, *et al.*, "A 10-bit charge-redistribution ADC consuming 1.9 μW at 1 MS/s," *IEEE J. Solid-State Circuits*, vol. 45, no. 5, pp. 1007–1015, May 2010.

[17] M. Miyahara, *et al.*, "A 2.2 GS/s 7 b 27.4 mW time-based folding-flash ADC with resistively averaged voltage-to-time amplifiers," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2012, pp. 388–389.