A 77dB SNDR 12.5MHz Bandwidth 0-1 MASH ΣΔ ADC Based on the Pipelined-SAR Structure

Yan Song[1,2], Yan Zhu[1], Chi-Hang Chan[1], Li Geng[2] and Rui Paulo Martins[1,3]
[1]State-Key Laboratory of Analog and Mixed Signal VLSI, DECE/FST, University of Macau, Macau, China; yansong@ieee.org
[2]School of Microelectronics, Xi'an Jiaotong University, Shaanxi, China
[3]On leave from Instituto Superior Técnico, Universidade de Lisboa, Portugal

Abstract

This paper presents a wide-band and energy-efficient 0-1 MASH ΣΔ ADC which is realized based on the pipelined-SAR structure. Composed by a 6b SAR ADC in the 1st-stage and a 5b SAR ADC in the 2nd-stage, with alternate loading capacitors (ALC) reused for error feedback, it realizes an ideal 1st-order noise shaping while simultaneously maintaining a high-speed pipeline operation. Fabricated in 65nm CMOS, the prototype consumes 4.5mW from a 1.2V supply with 77dB SNDR over 12.5MHz bandwidth, leading to a 171.5dB Schreier FoM.

Introduction

Wideband, high-resolution and energy-efficient ADCs are in high demand for mobile communications and IoT systems. Noise-shaping (NS) SAR [1][2] and SAR+VCO-based ΣΔ ADCs [3] have demonstrated a promising result in the resolution ~75dB SNDR but with a limited bandwidth (BW) of < 5MHz. Such limitation lies in their NS mechanisms where the residual voltage from the SAR ADC needs to be kept available until the completion of the whole conversion. Besides, although passive NS SAR ADCs [4][5] are inherently robust under process variations due to the switched-capacitor passive integrator, their NS efficiency is degraded by the passive integration, limiting the achievable resolution to be < 70dB in wideband designs. While such efficiency can be improved by cooperating with a dynamic amplifier [2] or VCO [3], the gain variation under different process corners either affects the NTF or causes noise leakage, respectively.

This work presents a high-resolution and wideband 0-1 MASH ΣΔ ADC. An ideal 1st-order NS is realized through the proposed alternate loading capacitors (ALC) for error feedback, without experiencing any residual voltage attenuation, thus achieving a good noise shaping efficiency. Unlike previous arts, the 1st-stage ADC in the proposed architecture can be released for sampling and conversion during the 2nd-stage integration thus enabling the pipeline operation to achieve a bandwidth (BW) as high as 12.5MHz. While the accuracy of the NTF and noise cancellation filter only rely on the capacitor ratio, they are robust under process variation. We measured 6 samples of the prototype, implemented in 65nm CMOS, where their SNDRs only vary less than 0.3dB from 77dB without any gain calibration.

Proposed 0-1 MASH ΣΔ ADC

Fig. 1 shows the basic block diagram of the proposed 0-1 MASH ΣΔ ADC. A single-ended structure is presented here for simplicity, while the actual implementation is fully differential. The ADC is modified from the conventional 10b pipelined-SAR structure. With 1b overlapping between the stages, an error < 64 LSBs from the coarse quantizer can be covered. The quantization error of the 1st-stage (E_H) is amplified by G times through the residue amplifier and transferred to the 2nd-stage. While the quantization error of the 2nd-stage (E_L) of the previous sample passes through a loop filter ($H(z)$) and adds to

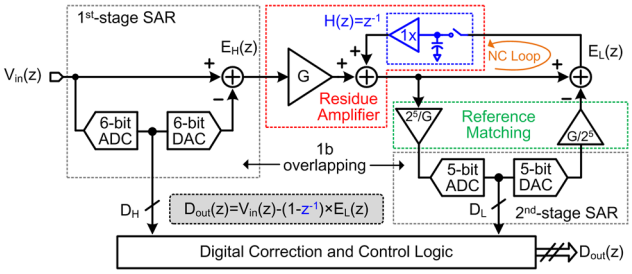

Fig. 1 Block diagram of the proposed 0-1 MASH ΣΔ ADC.

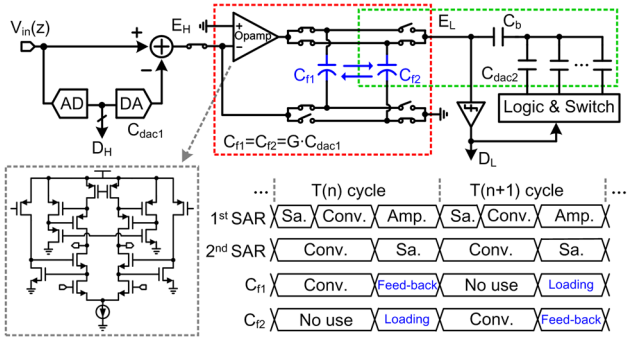

Fig. 2 Schematic and timing sequence of the proposed ADC.

the amplified E_H ($G \times E_H$). Then, their sum is further quantized by the 2nd-stage coarse ADC. With $H(z)=z^{-1}$, we accomplished a noise coupled (NC) loop leading to a 1st-order NS effect on E_L.

Conventionally, if two stages are implemented with the same reference voltage, an inter-stage gain of 2^5 is required. However, it is preferred to have smaller G to relax the linearity of the residue amplifier, thus we introduce a reference matching block with gain of $2^5/G$ to compensate the low G before the A/D conversion, avoiding noise leakage. In order to obtain the correct E_L for the proper NC function, we added an attenuation factor of $G/2^5$ after the D/A conversion. Unlike previous designs [1]-[3], where the NTFs are affected by the gain ratio between the forward signal and the feedback residue voltage, the accuracy of the NTF in our design only relies on the gain of the NC loop. Since the gain of the NC loop is defined by the capacitor ratio here, the achieved NTF is robust under process variation.

Fig. 2 shows the simplified circuit schematic and timing diagram of the proposed architecture. The modulator with ALC can be realized by simply reconfiguring the conventional pipelined-SAR structure without additional area overhead. Conventionally, during the residue amplification phase, C_{f1} and the parallel connected C_{f2} and C_{dac2} act as the feedback and loading capacitor of the opamp, respectively, where C_{f2} also serves as the gain attenuation in the reference matching block. After the 2nd-stage conversion, E_L is left on the top-plate of C_{f2}. Thus, C_{f2} can be re-configured as the feedback capacitor to

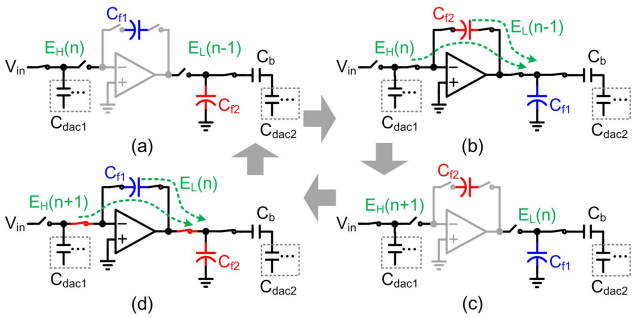

Fig. 3 Circuit operation of the ALC (a) sample and conversion, (b) C_{f2} feedback and C_{f1} loading, (c) next sample and conversion, (d) C_{f1} feedback and C_{f2} loading.

realize the error feedback of E_L without any voltage attenuation in the next residue amplification phase. Such configuration not only provides a buffer (1x) and delay (Z^{-1}) function of $H(z)$, but also realizes an inter-stage gain of G together with C_{dac1}. Meanwhile, C_{f1} can be re-configured as the loading capacitor and samples the output voltage of the opamp together with C_{dac2}. With the proposed ALC technique, we complete the NC loop without affecting the operation of the pipelined-SAR structure. Nevertheless, with conventional setup, the size of C_{dac2} is restricted by C_{f2} corresponding to the reference matching factor ($G/2^5$). To relax such constraint, a bridge DAC structure is utilized which isolates C_{dac2} and C_{f2} with C_b, thus allowing the size of C_{dac2} to shrink in order to save power and area. The residue amplifier is implemented with a gain-boosted cascode structure. With a typical mismatch σ=0.1% in our custom-designed MoM unit capacitor, the residue amplification and the reference matching blocks have a maximum total gain variation of 0.2, leading to only 0.5dB variation of the SNDR. Besides, thanks to the close loop structure, the proposed design has a better supply and common-mode rejection performance than prior-arts [2][3].

Fig. 3 shows the detailed switching sequence of C_{f1} and C_{f2} with the proposed ALC technique. First, the two stage ADCs sample the input and perform conversion. The $E_L(n\text{-}1)$ of the previous sample is left on the top-plate of C_{f2} when conversion finishes. In the residue amplification phase, C_{f2} is connected between the input and output of the amplifier, while C_{f1} and the series connected C_b and C_{dac2} are configured as loading capacitors. Both the voltages of $G\times E_H(n)$ and $E_L(n\text{-}1)$ are transferred to the top-plate of C_{f1}. Then the sum is further quantized by the 2nd-stage ADC, while the 1st-stage ADC continues a new sample and conversion of V_{in}. In the following residue amplification phase, C_{f1} and C_{f2} exchange their roles and finally achieve the 1st-order NS effect.

Measurement Results and Conclusion

Fig. 4 (left) shows the measured 32768-point FFT spectrum, with f_S=200 MS/s and f_{in}=1.5 MHz, of the proposed 0-1 MASH ΣΔ ADC, fabricated in 65nm CMOS. Capacitor mismatches are calibrated through LMS estimation [6] offchip. The proposed ADC achieves a SNDR of 77.1 dB over 12.5 MHz BW. Fig.4 (right) exhibits the measured SNR and SNDR over 6 chip samples which are stable without any gain calibration. Fig. 5 presents the SNR & SNDR versus the input amplitude and the OSR at 1.5 MHz input frequency. Due to the noise floor, the SNR increases about 7 dB when the OSR doubles (with small OSRs), indicating an ideal 1st-order NTF in our prototype.

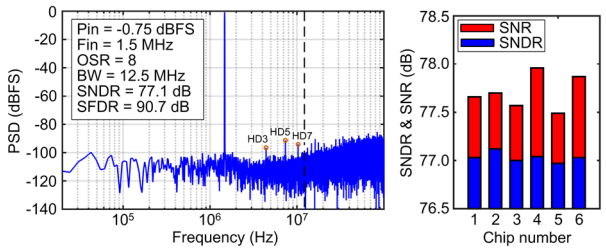

Fig. 4 Measured FFT spectrum and SNDR/SNR over samples.

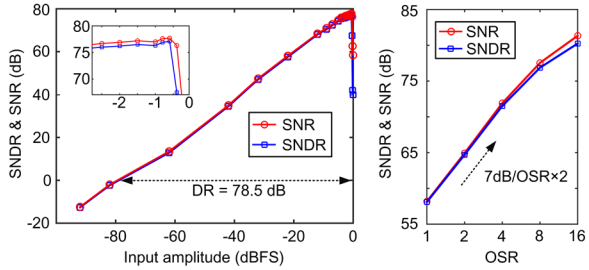

Fig. 5 Measured SNDR & SNR vs. input amplitude and OSR.

TABLE I. PERFORMANCE COMPARISON

Specifications	VLSI 17 [1]	ISSCC17 [2]	VLSI 16 [3]	VLSI 17 [4]	This work
Architecture	PNS SAR	PNS SAR	SAR VCO	PNS SAR	NS Pipeline SAR
Technology (nm)	40	28	40	14	65
Supply (V)	1.1	1.0	1.1	1.0	1.2
Fs (MHz)	8.4	132	36	300	200
BW (MHz)	0.262	5	2	25	12.5
SNDR (dB)	80.0	79.7	74.3	69.1	77.1
Power (mW)	0.143	0.46	0.35	2.4	4.5
FoMs (dB)	172.6	180.1	171.9	169.0	171.5
Area (mm^2)	0.04	0.0049	0.03	0.0043	0.014

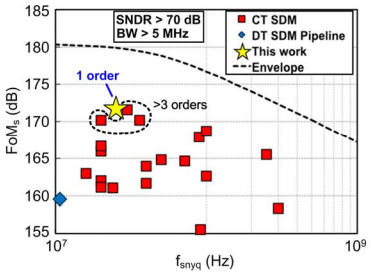

Fig. 6 Performance comparison

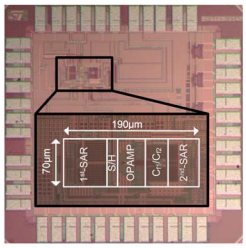

Fig. 7 Chip micrograph

Table I summarizes the ADC's performance and compares it with prior arts. This work achieves the highest BW among the NS SAR/SAR-assisted type ADCs with a SNDR>75 dB. Comparing with other ADCs under similar performance in Fig. 6 this design demonstrates a competitive Schreier FoM of 171.5 dB with accurate loop coefficient while others in the continuous-time (CT) need an additional tuning circuit for the time constant of the RC replica. The chip micrograph is shown in Fig. 7 where the ADC occupies 0.19 × 0.07 mm^2.

Acknowledgements

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