28.5 A 0.2V Energy-Harvesting BLE Transmitter with a Micropower Manager Achieving 25% System Efficiency at 0dBm Output and 5.2nW Sleep Power in 28nm CMOS

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Massive deployment of wireless sensor tags (e.g. iBeacon) will only happen if batteries and their replacement effort are avoided. Self-powering by harvesting the ambient energies like indoor solar and thermal gradient is prospective [1], but their inconstant sub-0.5V output hinders their utility. Adding boost converters and regulators inevitably worsens the system efficiency and integration level. This paper reports an energy-harvesting Bluetooth Low-Energy (BLE) transmitter (TX) (Fig. 28.5.1). It features a fully integrated micropower manager (μPM) to limit the sleep power and tolerate variation of the energy-source voltage ($V_{DD,EH}$) down to 0.2V. U=An ultra-low-voltage (ULV) VCO and PA, and a passive-intensive type-I PLL are proposed. Fabricated in 28nm CMOS, the TX exhibits a 25% system efficiency at 0dBm output (P_{out}).

The TX (Fig. 28.5.1) tailors a μPM with 4 specific charge pumps (CP_{1-4}) to deliver the internal power and bias. CP_1 is capable to self-start since $V_{DD,EH}$=0.2V. It generates a 1V $V_{DD,PM}$ to power-up the bandgap reference (BGR). CP_1 and BGR together offer $V_{DD,PM}$ and PVT-insensitive $V_{REF,PM}$ (0.55V) to start and operate CP_{2-3}. Since the VCO plus PA dominate 99% active power, ULV designs allow them to operate directly under $V_{DD,EH}$ (energy harvester + storage). Both VCO and PA are biased with a stable V_{BIAS} (0.39V) given by the BGR to resist $V_{DD,EH}$ variation. The passive-intensive type-I PLL draws only 54μA from a 0.55V $V_{DD,PLL}$ offered by CP_2. Static logic controls are under 1V $V_{DD,CTRL}$ given by CP_3. To inhibit the sleep power, a sub-nW always-on CP_4 is employed to generate a –0.17V V_{NEG} for power-gating the VCO and PA.

Only CP_1 of the μPM is detailed (Fig. 28.5.2). A switched-capacitor rectifier driven by a multiphase ring-VCO reduces the switching ripple at $V_{DD,PM}$, which otherwise calls for a big C_{de} compromising the area and startup time. The ring-VCO, using differential bootstrapped inverters, secures an adequate output swing (ideally $3\times V_{DD,EH}$) to drive the rectifier without extra buffers. To cope with $V_{DD,EH}$ variation, the error amplifier senses $V_{DD,PM}$ and adjusts the delay lines of the ring-VCO via V_{DL}. Thus, its oscillation frequency can be moderated to limit the excessive power when $V_{DD,EH}$ raises. The forward diodes at $V_{DD,PM}$ are for overdrive protection.

CP_{2-3} (not shown) are similar to CP_1, but their error amplifier directly locks the bias current of the ring-VCO, so as to regulate $V_{DD,PLL}$ and $V_{DD,CTRL}$ [1]. The always-on CP_4 is based on a negative-output rectifier driven by a kHz-range ring-VCO. In the μPM measurement (Fig. 28.5.2), the critical voltages are stabilized against $V_{DD,EH}$=0.2 to 0.3V, and settle in <400μs that can be overlapped with the startup time of the crystal oscillator [1].

The trifilar-coil VCO [2] features a large passive loop gain to facilitate startup at ULV. Yet, the VCO steady-state power consumption is decided by both the loss of the LC tank and transistor channel conductance (G_{DS}). Since the trifilar-coil VCO has out-phased V_{GS} and V_{DS}, its cross-coupled pair is pushed into the triode region, resulting in large G_{DS} and power consumption especially at ULV. Here, our ULV VCO (Fig. 28.5.3-left) removes the drain-to-gate feedback for a constant drain voltage V_D of $M_{1,2}$ set by $V_{DD,EH}$. Differential-mode oscillation is achieved by source-to-gate magnetic cross-coupling (V_{S-} to V_{G+} and V_{S+} to V_{G-}). Unlike [3], an auxiliary cross-coupled pair is not entailed at the gate, which otherwise penalizes the phase noise (PN) by ~2dB in the $1/f^2$ region (even with a size of one-tenth of $W/L_{M1,2}$). Since V_{G+} and V_{S+} (V_{G-} and V_{S-}) are in-phase, they lead to a large $|V_G|$ (~$0.78V_{pp}$) improving the PN, and can serve as the VCO outputs. The reduced V_{GS} (~$0.51V_{pp}$) helps $M_{1,2}$ to stay in the saturation region, avoiding Q degradation of the transformer.. The transformer has a primary coil ($L_{A11,12}$) stacked atop its secondary coil ($L_{A21,22}$) to enlarge both the coupling factor (k_A≈0.76) and turns ratio ($N_{GS} = 5.6 = \sqrt{L_{A11}/L_{A21}}$). The VCO hence shows a large passive loop gain proportional to $k_A N_{GS}$ even in the presence of source degeneration. In active mode, $M_{1,2}$ has a gate bias V_{BIAS} (0.39V) given by the BGR that further facilitates startup at ULV. DC isolation between V_{GB} and $V_{DD,EH}$ improves the frequency pushing (measured 29.7MHz/V).

The 2.4GHz VCO outputs ($V_{G\pm}$) directly drive the ULV PA (Fig. 28.5.3-right) that operates in the Class-E/F_2 mode to enhance the power efficiency. To meet a 0-dBm P_{out} at 0.2V, we exploit a step-down transformer ($L_{B1,2}$) to reduce the drain-node resistance of $M_{3,4}$, while rejecting the even-order harmonics at V_{out}. To suppress the HD_3 without adding an explicit LC filter, C_n (0.7pF) is embedded into the secondary coil (L_{B2}) to resonate with a part of its inductance (L_n) at 3× of the 2.4GHz ISM band: $3f_0 = 1/(2\pi\sqrt{L_nC_n})$. As such, $|Z_{22}|$ of the PA will present a high impedance at $3f_0$ to obstruct the 3rd-harmonic current. L_n is routed as the most inner 2 turns of L_{B2} (Fig. 28.5.7), with its dimension (D_1) being designed to balance the HD_3 and PA efficiency. Simulations suggest that D_1=100μm aids balancing HD_3 (–47 dBm) and PA efficiency (30.6%) at P_{out}=0dBm. Comparing with no L_nC_n, HD_3 is rejected by 19dB more (Fig. 28.5.3-right). The passband loss rises only 0.5dB, since the magnetic coupling between L_{B1} and L_{B2} is dominated by their outer turns. In sleep mode, the shared gate bias (V_{BIAS}) of the VCO ($M_{1,2}$) and PA ($M_{3,4}$) is switched to V_{NEG} (–0.17V) optimized for leakage power reduction (measured 4.9nW). The VCO can be switched to the receiver mode by shutting down the PA via SW_{PA}.

The VCO is locked by a type-I integer-N PLL with $V_{DD,PLL}$=0.55V, and f_{REF}=1MHz to support channel selection (Fig. 28.5.4). With a passive XOR gate + an inverter-based buffer, V_x is rail-to-rail pulses and hence a 0-to-0.55V V_{CTRL} range for frequency tuning is realized. Unlike [4] that uses 50%-duty-cycle $\phi_{1,2}$ to drive the master-slave sampling filter (MSSF), here ϕ_1 utilizes a 10× less duty cycle (i.e. 5%) to reduce the ripple of V_{CTRL} mainly induced by the clock feedthrough from V_A, which aids in suppressing the reference spur. It can be quantified by analyzing the 1st-harmonic Fourier coefficient of V_{CTRL}. Meanwhile, the XOR gain varies with V_{CTRL}, and has a simulated minimum gain improved from ~0.03 (50% ϕ_1) to 1.21V/rad (5% ϕ_1), which expands the loop bandwidth to better suppress the VCO PN. During open-loop FM modulation, S_1 is off and S_2 is on. Thus, $C_{1,2}$ are in parallel (26pF) to reduce the V_{CTRL} leakage. The swing of $\phi_{1,2}$ is bootstrapped to lower the size of $S_{1,2}$ (transmission gates). The PLL excluding the VCO dissipates 30μW mainly for the divider.

The TX fabricated in 28nm CMOS satisfies the strict minimal density rules. Under open-loop modulation, the TX shows a system efficiency of 25% at P_{out}=0dBm and $V_{DD,EH}$=0.2V, and 27% at P_{out}=3.7dBm and $V_{DD,EH}$=0.3V (Fig. 28.5.5). A single-tone P_{out} of 0dBm shows HD_2=–49.6dBm and HD_3=–47.4dBm. The BLE spectral mask is met and FSK error is just 2.2%. The frequency drift is <5kHz when delivering a 425μs BLE packet. The free-running VCO shows a FOM of 188.4dB at 1MHz offset, and a $1/f^3$ corner at 150kHz. The PLL+VCO power efficiency is 0.29mW/GHz, and the largest spurs are –47dBc. The settling time measures 30 at an initial frequency offset of 30MHz. The complete TX has a sleep power of 5.2nW and active area of 0.53mm^2 (Fig. 28.5.7).

Benchmarking with the recent art [4-6] in Fig. 28.5.6, this work achieves a BLE TX μPM that enables ULV operation down to 0.2V, while upholding a high system efficiency and full integration. [5-6] use dual supplies, and their performances have not included the loss, power and area of the power-management units. [7] aims at direct battery operation.

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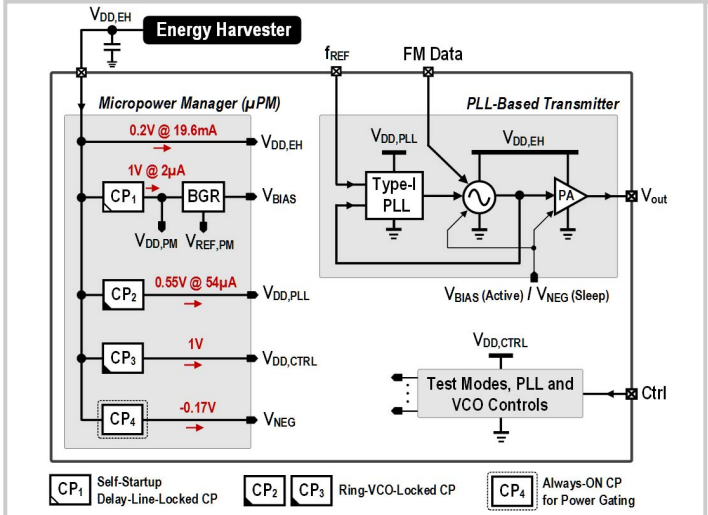

Figure 28.5.1: Proposed energy-harvesting BLE TX features a fully-integrated μPM to control the active/sleep power and tolerate variation of the energy source ($V_{DD,EH}$) down to 0.2V.

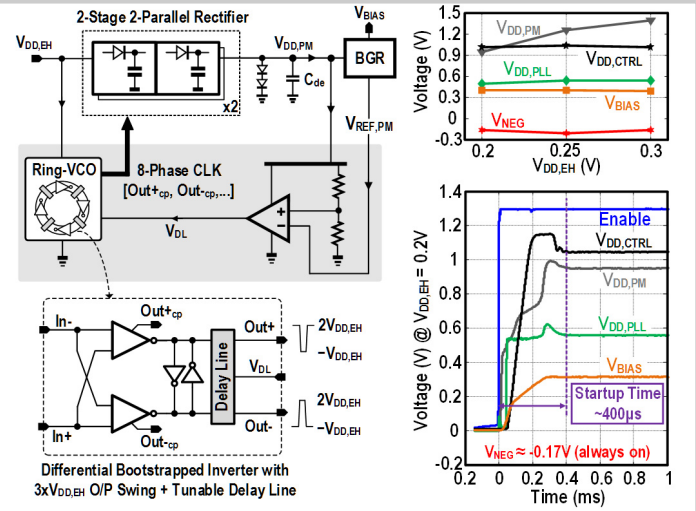

Figure 28.5.2: Left: CP_1 of the μPM. Its ring-VCO is locked via tunable delay lines to track $V_{DD,EH}$ variation. Right: Measured internal voltages against $V_{DD,EH}$ and their startup time.

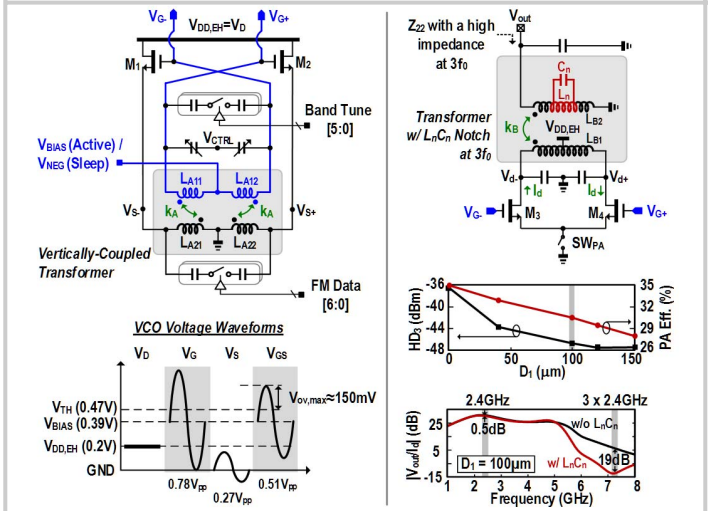

Figure 28.5.3: Left: ULV VCO with $M_{1,2}$ always in saturation region even at $V_{DD,EH}$=0.2V. Right: ULV Class-E/F_2 PA, with its transformer-embedded L_nC_n notch to suppress HD_3

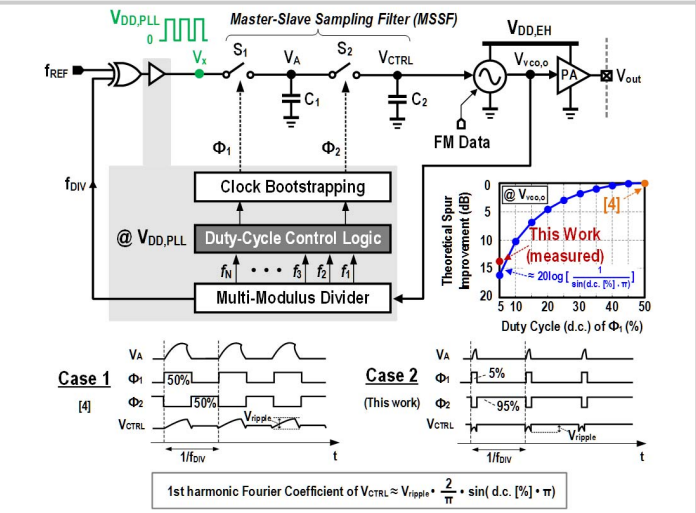

Figure 28.5.4: A 2.4GHz integer-N type-I PLL with passive XOR and MSSF. The MSSF uses a 5%-duty-cycle Φ_1 to aid suppressing the reference spurs. $V_{DD,PLL}$=0.55V and f_{ref}=1MHz.

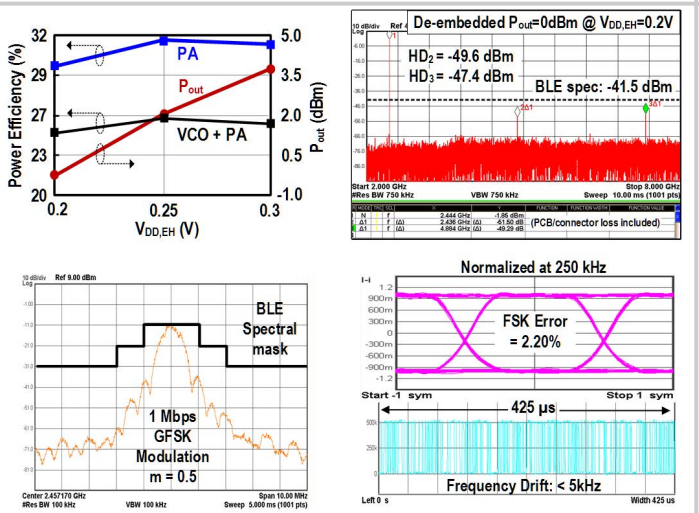

Figure 28.5.5: Upper: measured P_{out}, power efficiency and $HD_{2,3}$. Lower: measured modulated output spectrum, FSK error and frequency drift under open-loop operation.

Parameters	This Work	JSSC'16 [5]	JSSC'17 [6]	ISSCC'15 [7]
Key Techniques	μPM + ULV VCO & PA + Type-I Analog PLL	Dual-V_{DD} + Class-E/F_2 PA + LC-DCO + ADPLL	Dual-V_{DD} + Function-Reuse DCO-PA + ADPLL	Class-D PA + LC-DCO + ADPLL
CMOS Technology	28 nm	28 nm	65 nm	40 nm
Active Area (mm^2)	0.53 *	0.65	0.39	0.6
O/P Matching Network	Fully On-Chip	Fully On-Chip	Partially On-Chip	Partially On-Chip
HD_2/HD_3 @ P_{out} (dBm)	−49.6 / −47.4 @ 0 dBm	−50 / −47 @ 0 dBm	−43.2 / −47.6 @ 0 dBm	−49 / −53 @ −2 dBm
Modulation Error	2.2% (GFSK)	2.7% (GFSK)	2.29% (HS-OQPSK)	4.8% (GFSK)
Supply Voltage (V)	0.2	0.5 (DCO) 1 (ADPLL & PA)	0.4 (DCO-PA) 0.7 (ADPLL)	1
TX Power Consump. (mW) @ P_{out}	4 @ 0 dBm *	3.6 @ 0 dBm	4.4 @ 0 dBm	3.45 @ −2 dBm
TX Power Efficiency (%) @ P_{out}	25 @ 0 dBm *	28 @ 0 dBm	22.6 @ 0 dBm	18.3 @ −2 dBm
Sleep Power (nW)	5.2	N/A	N/A	N/A
VCO PN @ 1MHz offset (dBc/Hz)	−119	−116 to −117	−116	−110
VCO FoM @ 1MHz offset (dB)	188.4	188 to 189	N/A	183
PLL Power Efficiency (mW/GHz)	0.29	0.57	N/A	0.39
PLL FoM #(dB) normalized @ 1MHz f_{ref}	-227.2	-231.6	N/A	-220.9
PLL Largest Spurs (dBc)	-47	-60	-42	-38

* Included a fully-integrated μPM. [5-7] have not included the loss, power and area of the power-management units.

$$\#\ \text{PLL FoM} = 10\log\left[\left(\frac{\sigma_{rms}}{1\ \text{sec}}\right)^2 \cdot \frac{\text{Power}}{1\ \text{mW}} \cdot \frac{f_{REF}}{1\ \text{MHz}}\right]$$

Figure 28.5.6: Benchmark with the recent art. This work and [5-7] use open-loop modulation.

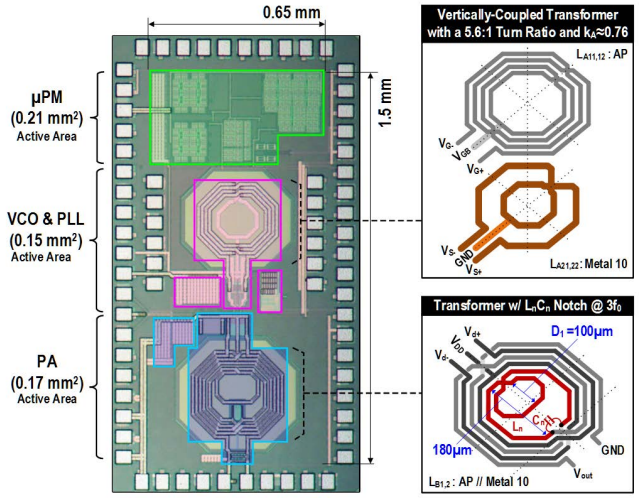

Figure 28.5.7: Die micrograph of the 28nm CMOS BLE TX and details of transformers. Extra pads are for individual characterization of the μPM, VCO and PA in active and sleep modes.

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